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Volume 29, Number 2

March • April 2025

Glass-based interposer for co-packaged optics

- New package solutions for automotive optical sensors
- Reliability challenge of underfills in large-size HI FO-MCM packages
- Impact of BGA solder metallurgy on BLR failure modes in FC packaging
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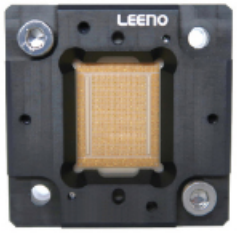

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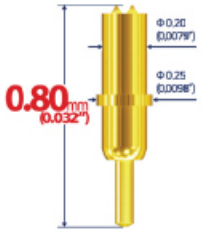

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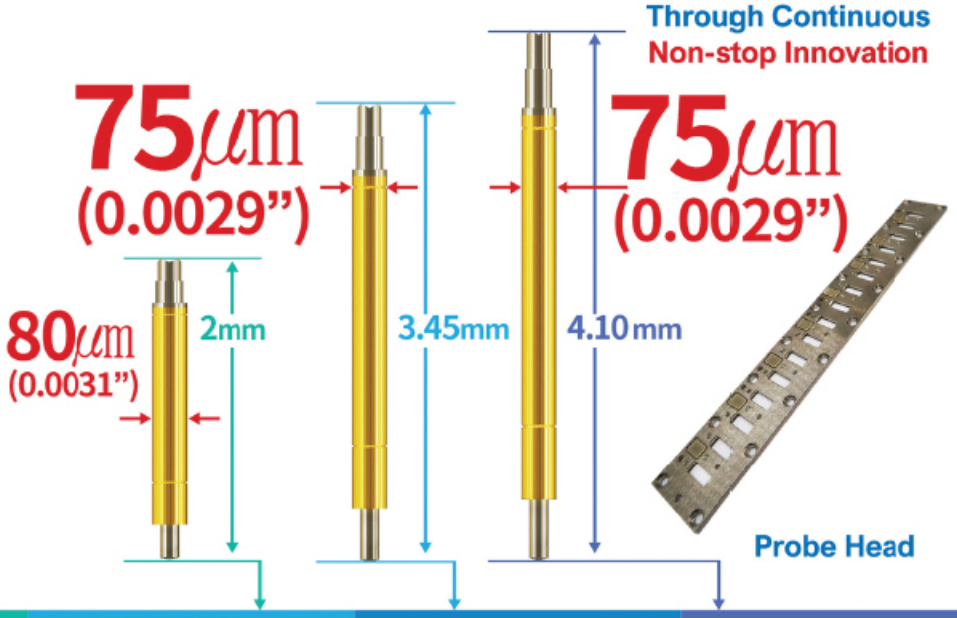

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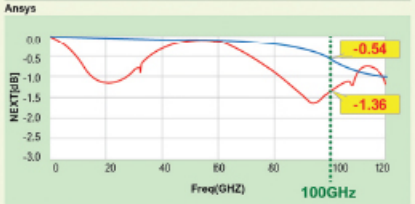

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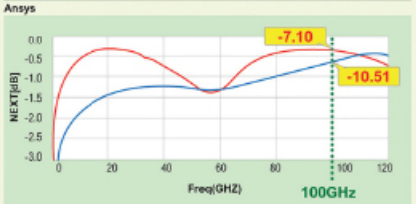

Crosstalk

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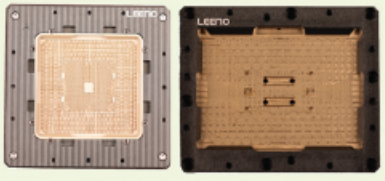

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CONTENTS

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Advanced packaging substrates, such as glass-based interposers combined with automated packaging processes, can overcome manufacturing bottlenecks in photonic component assembly.
This approach will enable photonic and electronic co-packaged subsystems to scale to large-volume production. As a result, mass market demands--including data center communications, artificial intelligence, sensing and diagnostics—will be addressed.
The cover image shows the packaging of a microlens array to a flip-chip assembled InP photonic integrated circuit on a glass electrical interposer with BGA contacts.
Cover photo courtesy of Tyndall National Institute

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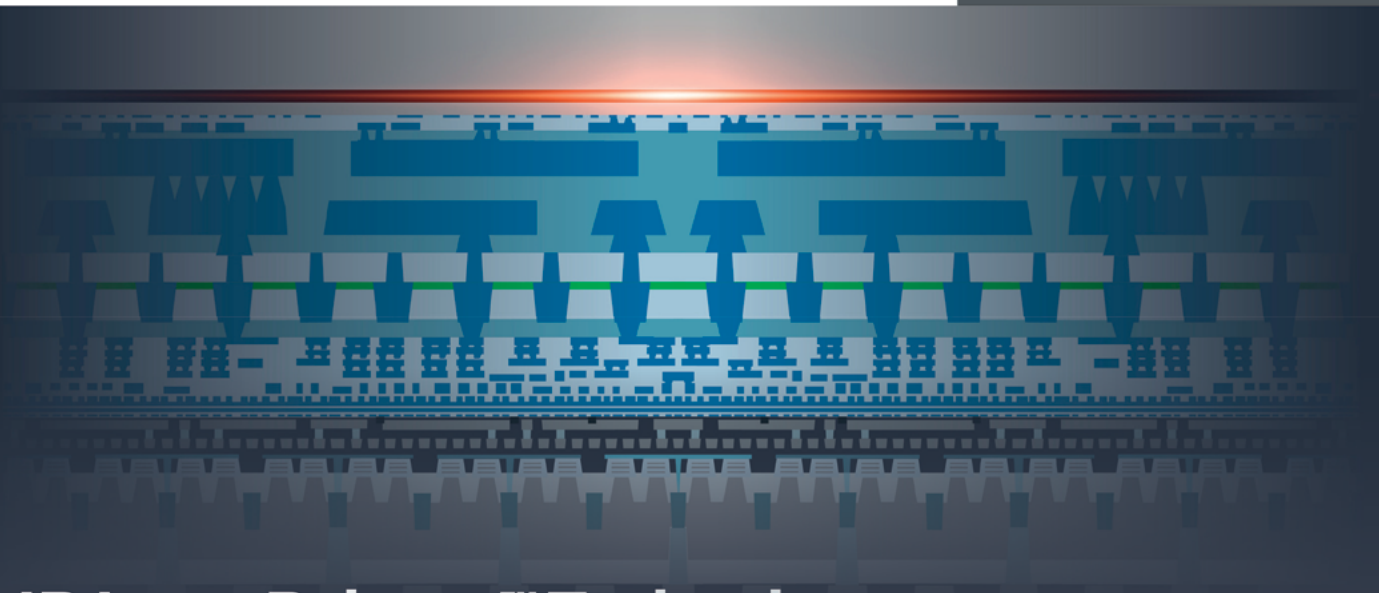

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CONTENTS

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STAFF
Kim Newman
Publisher
knewman@chipscalereview.com

Lawrence Michaels
Managing Director
Editor-in-Chief
lmichaels@chipscalereview.com

Debra Vogler
Senior Technical Editor
debravogler@me.com

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P.O. Box 2165
Morgan Hill, CA 95038
Tel: +1-408-846-8580
E-Mail: subs@chipscalereview.com

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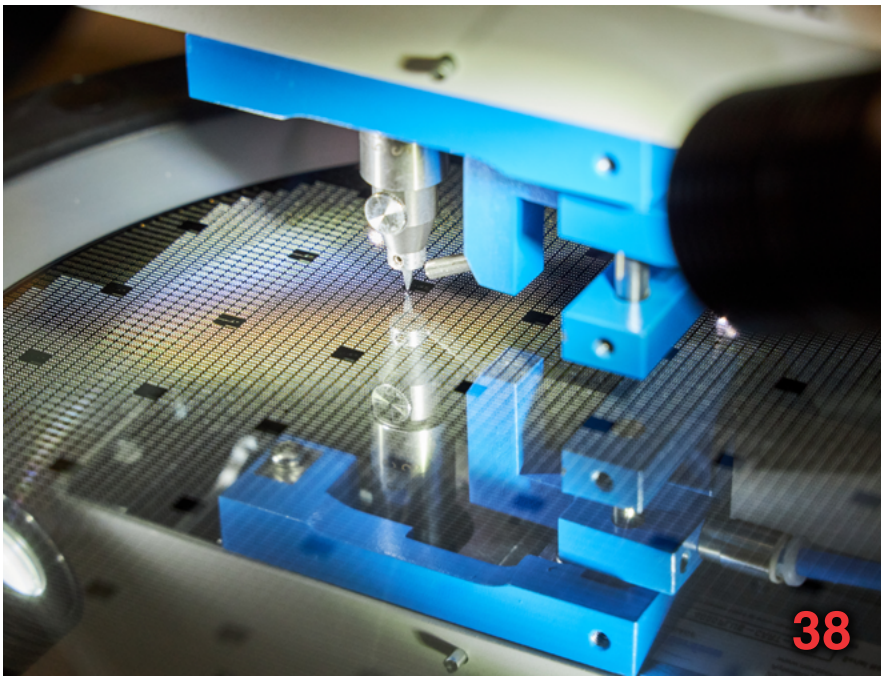

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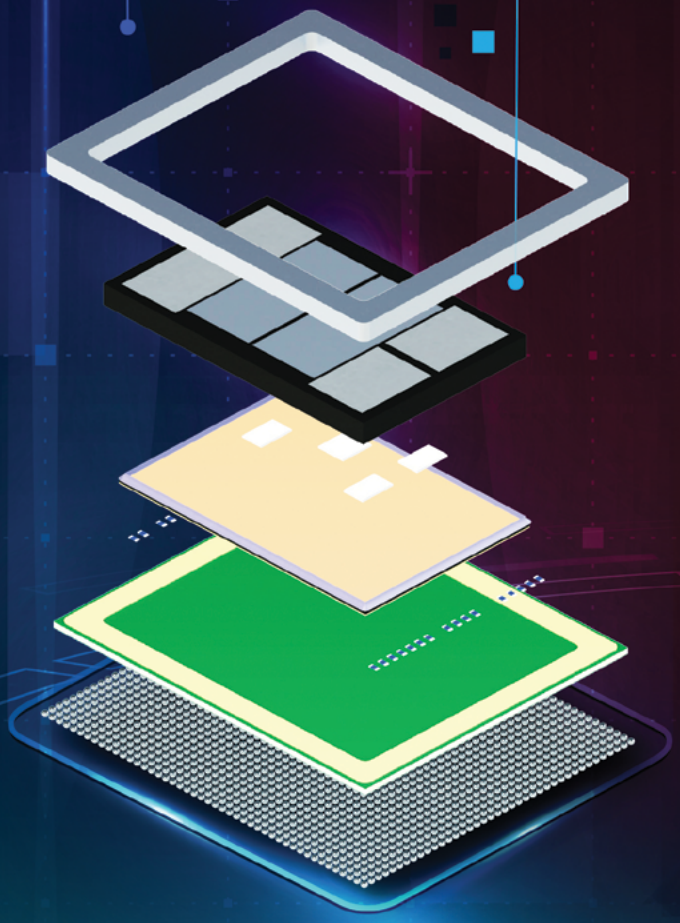

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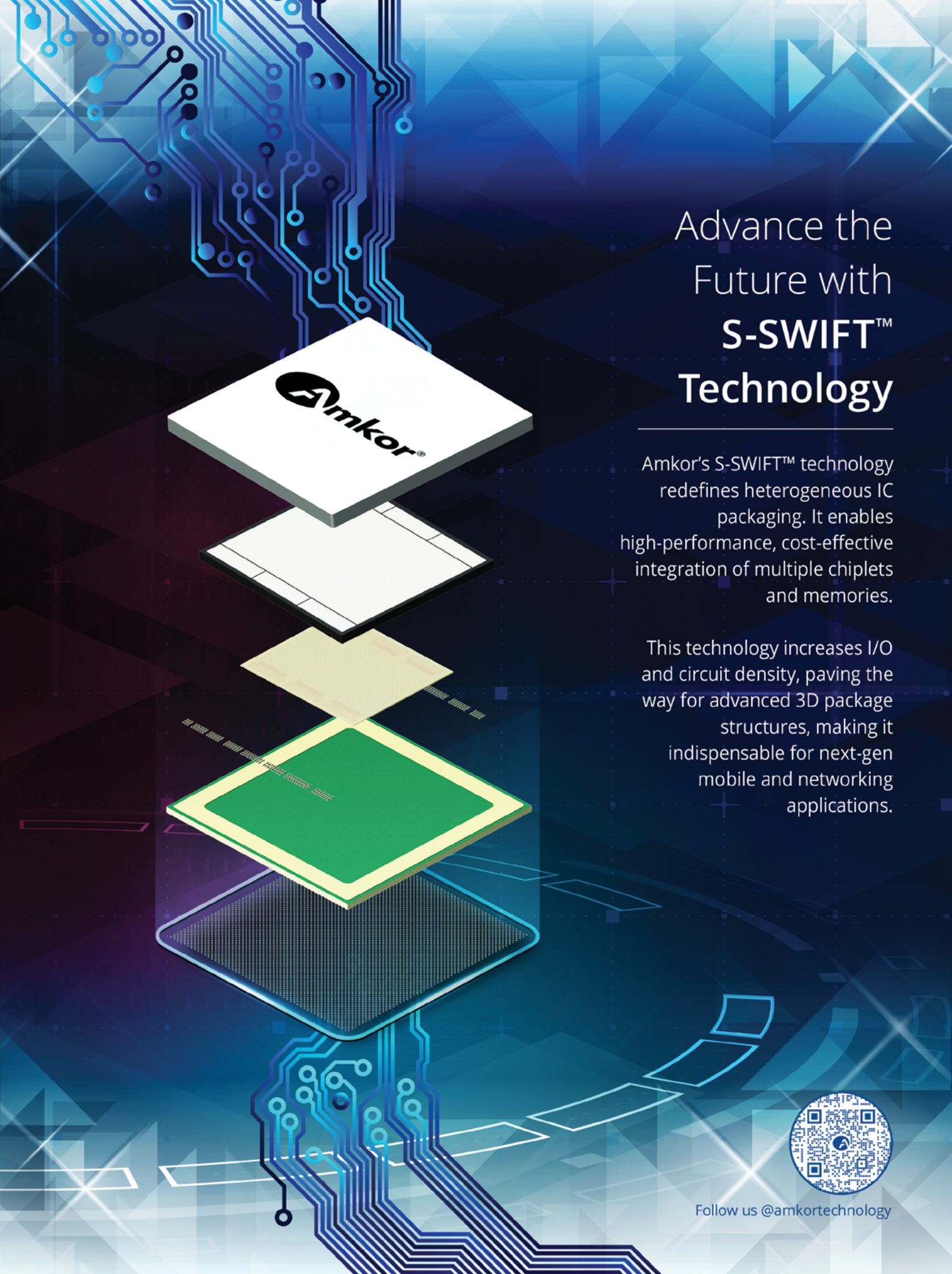

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Co-packaging of photonic and electronic ICs on glass interposers

By Peter O'Brien, Das Kumar [Tyndall National Institute]

As high-frequency communication, data centers and artificial intelligence (AI)-driven computing push the limits of existing technology, the need for advanced packaging solutions that efficiently integrate photonic and electronic components has never been greater. While silicon and organic interposers remain widely used, they struggle to meet the thermal and electrical demands of next-generation systems. In contrast, glass interposers offer a compelling alternative, delivering low radio-frequency (RF) loss, high thermal stability, and precise micro-structuring capabilities—critical factors for high-performance applications.

This article explores the co-packaging of photonic integrated circuits (PICs) and electronic integrated circuits (EICs) using glass interposers, leveraging through-glass vias (TGVs) to enable high-speed RF interconnects. Many of these developments have been achieved within the PhotonicLEAP project, funded by the European Commission under the Horizon Europe research program [1].

Building on advancements in flip-chip bonding, laser-assisted packaging, and free-space micro-optics integration [2], we introduce a fully glass-based photonic transceiver package designed for high-frequency applications. For photonic packaging to achieve widespread adoption, it must transition from early-stage research to scalable, cost-efficient manufacturing. This requires standardized design and assembly processes that align PICs, optical components, and packaging substrates. Equally important are advancements in automation and precision assembly, which will reduce costs and enable high-volume production of glass-based photonic systems.

Glass as a packaging material

Glass interposers are gaining popularity in IC packaging because of their unique material properties and advantages over traditional silicon and organic interposers. Glass interposers are increasingly recognized for their suitability in radio frequency (RF) and millimeter-wave (mmWave) applications, primarily due to their low loss tangent, which minimizes signal attenuation at high frequencies. This characteristic makes them ideal for advanced communication systems, including 5G and beyond.

Glass benefits from higher thermal stability making it suitable for high-power applications. It has a low coefficient of thermal expansion (CTE) and is comparable to that of silicon (~3.2ppm/K), thereby reducing thermal stress and warping. Incorporating TGVs into glass substrates significantly enhances local thermal conductivity. While unmodified glass typically exhibits a thermal conductivity around 1.2W/mK, the addition of TGVs can elevate this value to approximately 94W/mK. [3]. Consequently, integrating TGVs into glass interposers is a promising approach for managing thermal challenges in advanced electronic packaging. Furthermore, unlike organic materials, glass provides excellent dimensional stability, and bonding surfaces can be made flat to improve yield without additional fabrication steps.

Unlike silicon wafers, panel-level processing of glass would significantly scale up and reduce cost of manufacturability. In photonics packaging, optical properties of glass provide unique advantages where free space micro-optics and optical waveguides can be seamlessly integrated. Challenges include material brittleness, process maturity of TGVs, and complexity of integration with mainstream semiconductor packaging.

Glass wafer processing using LIDE

LPKF's laser-induced deep etching (LIDE) technology enables the micro-structuring of glass with the fabrication of precise, high-aspect ratio features without introducing defects such as micro-cracks or chipping. This innovative process consists of two key steps:

1. Laser modification, where specific regions within the glass substrate are selectively altered according to a predefined pattern.
2. The laser-modified areas (from step #1) are removed through a controlled wet chemical etching process, resulting in clean and highly-accurate microstructures.

Figure 1 shows the typical micro-structured hourglass, or V-shaped vias, in glass using the LIDE process. LIDE technology is compatible with standard silicate-based glasses and can produce features as small as 5µm, with

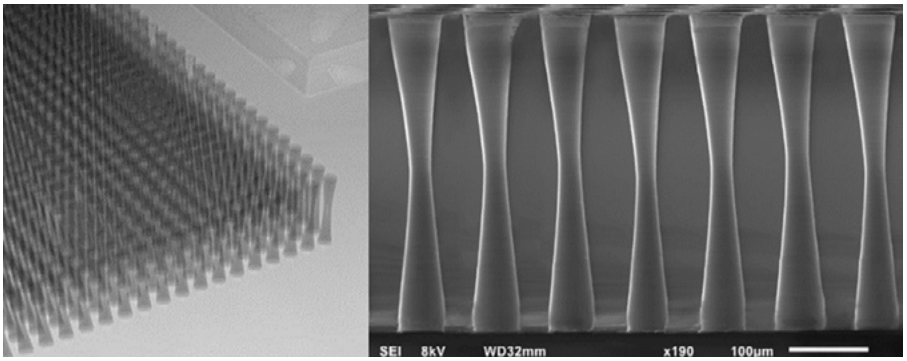


Figure 1: Hourglass shaped through-glass-via (TGV) using the LIDE process.

aspect ratios reaching 1:50. This makes it highly suitable for applications in semiconductor packaging, microfluidics, and display technology.

The following sections discuss glass wafer specifications and micro-hole/panel processing associated with using LIDE.

Glass wafer specifications. Glass interposers for multiple applications in the same wafer were designed using the LIDE process. BF33 (Schott) glass wafer material with a 200mm diameter and 0.5mm thick was used to fabricate the interposer. The TGVs have an aspect ratio of 1:10.

A standard cavity depth of up to (270±2)µm was achieved in the same wafer. The average TGV top and bottom diameters, measured using light microscopy, are calculated to be (50, 32±0.42)µm. Additionally, SEM cross-sectional analysis confirms a homogeneous hourglass TGV profile, consistent with the expected LIDE procedure. The average taper angle is (1.5±0.5)°.

Micro-hole and panel processing. The minimum via diameter achievable is 10µm, with uniform micro-hole diameters across a single substrate. The typical aspect ratio ranges from 1:10, but can reach up to 1:50, depending on the glass type. LIDE-generated micro-holes exhibit smooth, crack-free, chip-free, and stress-free sidewalls, ensuring reliable metallization. The taper angle varies between 0.1° and 30°. V-shaped micro-holes can be formed by restricting etching to a single side of the modified glass. Different via diameters can be achieved through multiple etching runs.

LIDE technology supports all standard wafer sizes, including 100mm, 150mm, 200mm, 300mm, and 450mm. However, panel formats are limited to dimensions below 510 × 510mm², and glass thickness is restricted to below 0.9mm.

Glass RDL design rules

With precisely-structured TGVs and cavities enabled by LIDE, glass wafers can serve as an ideal substrate for redistribution layers (RDLs) in advanced wafer-level packaging (WLP) applications. Figure 2 shows the essential design rules for RDLs in glass for WLP technology. Two RDLs on the top of the glass wafer are passivated by polyimide film.

Bond pads are metallized with Au. The height of the Au pillars can be set between 1µm up to 16µm, but is fixed throughout a single wafer. The hour-glass TGVs—with a nominal landing diameter of 50µm and waist diameter of 24µm—are filled with copper, and they route the topside RDLs to a single layer of backside RDL. A minimum L/S of 10µm applies on all RDLs. The ball grid array (BGA) pads are copper-nickel alloy and can be set to an arbitrary diameter with a minimum distance-to-via-pad (DTVP) of 20µm. The minimum via-landing-overhang (VLO) distance is 5µm and applies also to vias between RDLs. The minimum via diameter between topside RDLs is 35µm.

The following sections discuss various aspects of RDL design rules.

High-frequency characteristics on glass. Given the glass fabrication design rules, coplanar ground-signal-ground (GSG) transmission lines were designed and tested. Transmission lines with

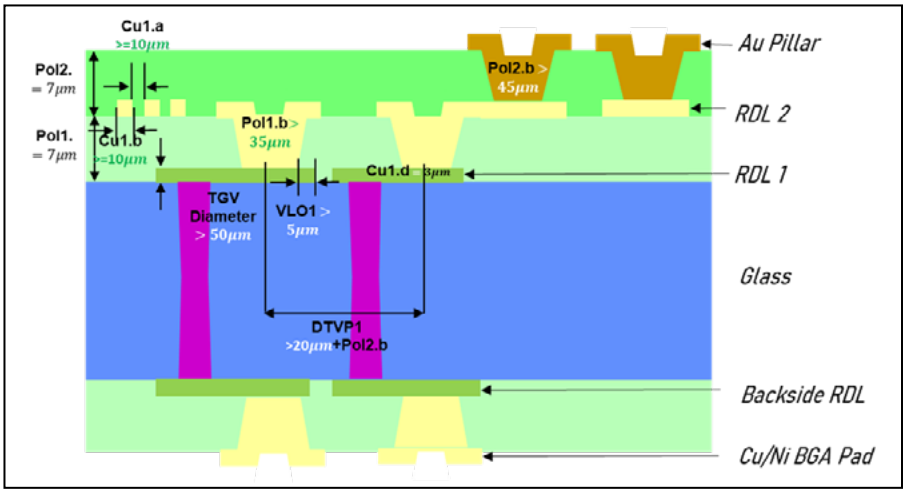


Figure 2: Design rules for redistribution layers (RDLs) in glass.

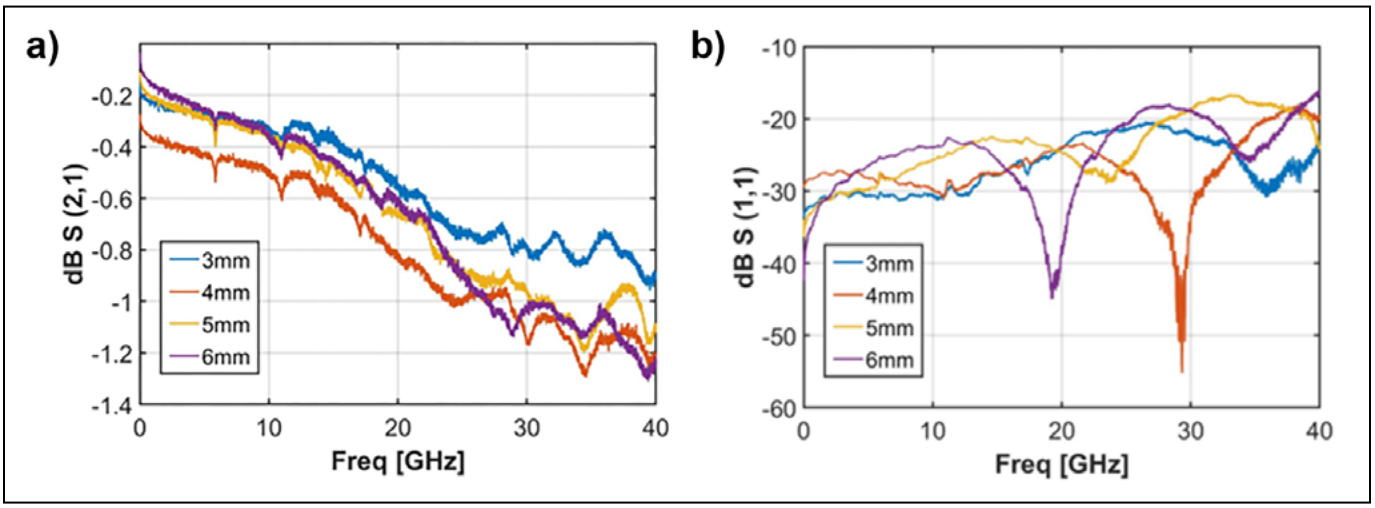


Figure 3: Measured S-parameter results with: a) S21, and b) S11, on GSG transmission lines up to a line length of 6mm on glass RDL 1.

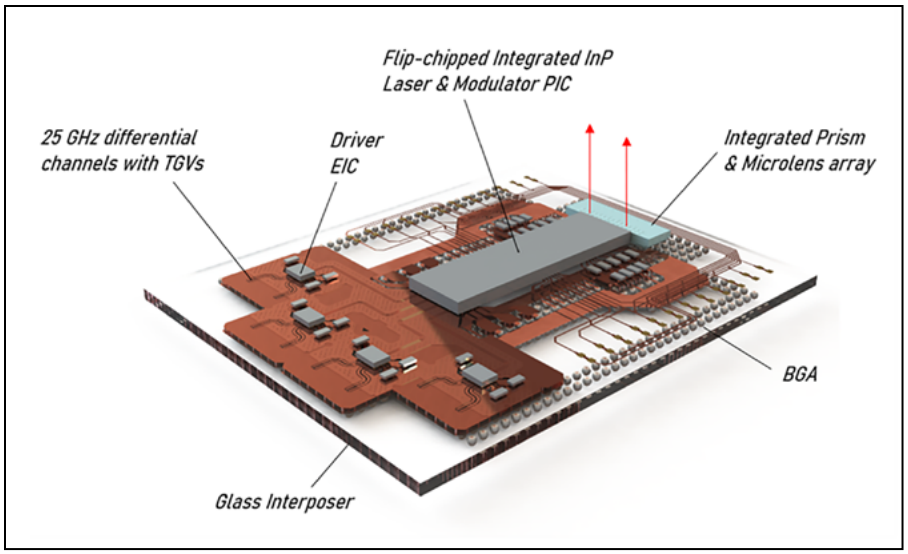


Figure 4: Glass interposer for a flip-chipped InP PIC along with four driver EICs. The package includes a custom microlens for out-of-plane coupling.

lengths of 3mm, 4mm, 5mm, and 6mm with a GSG configuration were fabricated on a glass wafer on RDL1 using design rules; results are shown in Figure 3. Simulation and measurement results of S21 and S11 were performed up to 40GHz and show excellent agreement, thereby validating the electrical parameters later used for the design to support 25GHz transceiver package-level operation.

Realized co-packaged transceiver using a glass interposer. Building on the electrical performance of glass-based interposers, a fully-integrated photonic-electronic package was developed to demonstrate the feasibility of high-speed signal transmission on a glass platform. The package incorporates an InP photonic integrated circuit (PIC) with four laser and modulator channels, operating at bandwidths up to 25GHz. These components are driven by differential RF signaling through a dedicated SiGe driver chip, thereby leveraging the high-frequency performance of glass RDLs and TGV interconnects.

The glass interposer design with the InP PIC and co-packaged driver EICs, capacitors, and the microlens array (MLA) is shown in Figure 4. The RF input is applied to BGA pins in the glass interposer. One hundred Ohm (i.e., 100 Ohm) differential ground-signal-signal-ground (GSSG) transmission lines were designed using TGVs to provide RF input channels to the driver EICs. The routing is made through the single RDL at the bottom, metallized TGVs, and double RDLs on top of the glass interposer following fabrication design rules.

The co-packaged EIC to PIC RF output channels are routed on the top two RDLs using an edge-coupled microstrip configuration; these lines are 50 Ohm differential GSSG transmission lines. Simulation (not shown here) results of these interconnects between co-packaged EICs and the PIC indicate a 1.25dB insertion loss at the 25GHz broadband operational frequency. The return loss is below -20dB per channel. In addition, alignment laser channels were incorporated to facilitate active alignment of the micro-optics on the flip-chipped PIC for out-of-plane coupling. The integrated prism and microlens array (prism and MLA) from FocusLight is constructed from silicon, and a cavity is designed on the glass interposer to house the microlens in the package.

PIC. The InP-based PIC consists of an array of four Mach-Zehnder modulators (MZMs) with an integrated laser source. The distributed feedback (DFB) laser sources are highly efficient, as both ends of a single laser feed into two separate modulators. The RF interface of the capacitively-loaded traveling wave electrode (TWE) of the MZM is positioned on the left side, while the optical interface is on the right, and the DC contacts are routed to the upper and lower sides of the chip. The electro-optical RF response of the modulator was measured up to 67GHz, with an electrical/optical 3dB bandwidth of 40GHz, exhibiting a gradual roll-off.

Figure 5 shows the InP PIC with two additional channels for the alignment lasers, in addition to the four laser/MZM channels. The additional channels are dedicated to the active and rapid alignment process of the optical MLA.

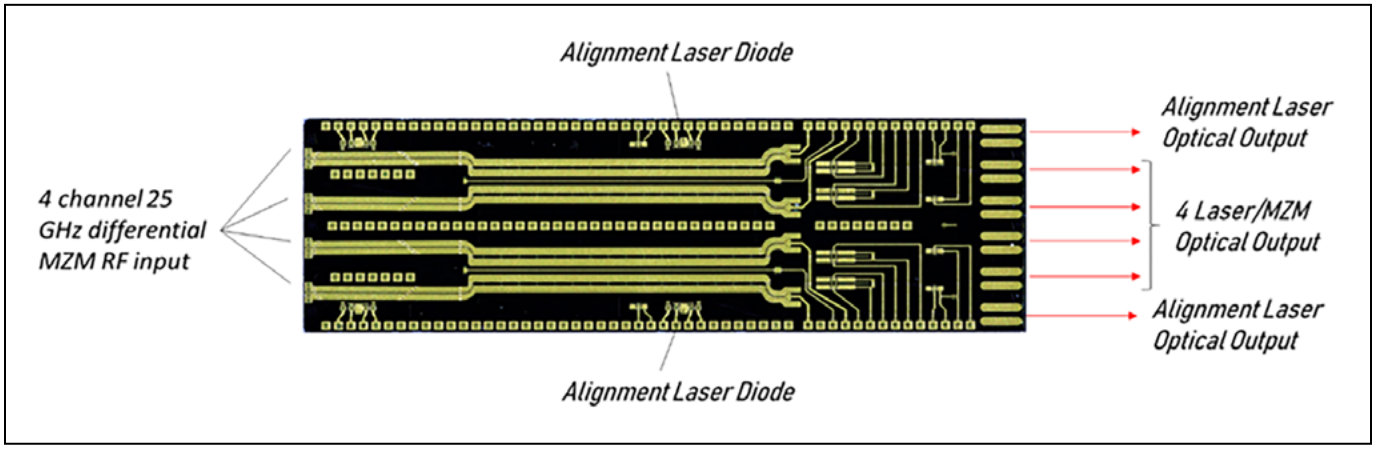


Figure 5: A flip-chip compatible InP PIC with integrated two alignment laser diodes, in addition to four laser and MZM channels. A differential signal applied to the MZM RF input enables 25GHz broadband operation in the package.

The four independent MZM channels are integrated with 2 × 25 Ohm RF termination resistors and laser sources each, operating at a wavelength of 1310nm. The measured mode-field diameter (MFD) of the edge coupler is asymmetrical, measuring 3.7µm in the x-direction (aligned with the chip's edge) and 2.9µm in the y-direction (vertical).

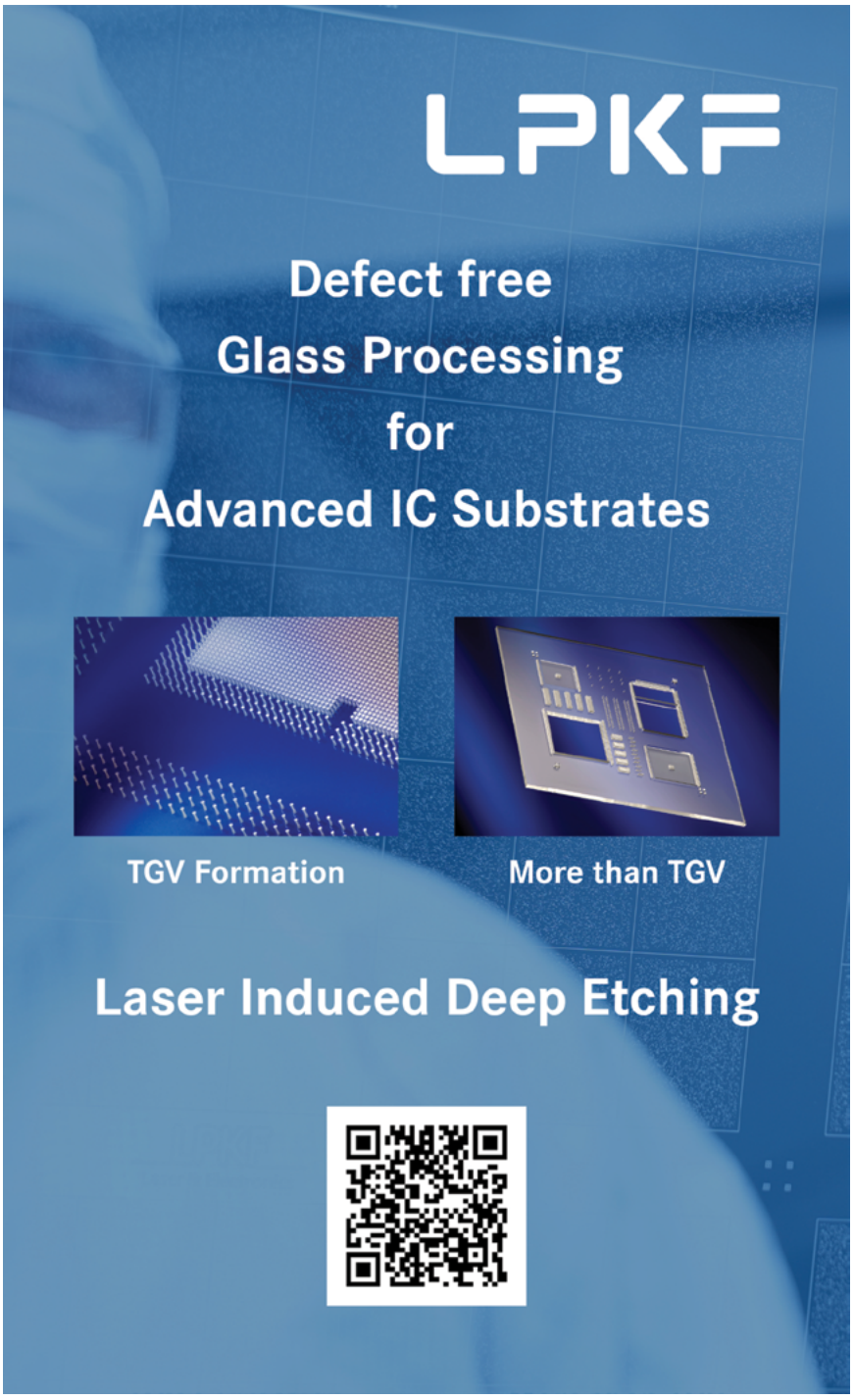
Driver EIC. The four MZMs of each PIC will be driven by individual driver electronic ICs (EICs). These driver EICs have been designed at FRN-HHI as ultra-low power SiGe 2-bit digital to analog converter (DAC) drivers for low-power high-bandwidth optical transmission systems. The EIC is co-designed and optimized with respect to FRN-HHI's InP-based MZM-modulator regarding impedance matching and signal integrity. By combining a DAC with the linear driver to generate PAM-4 signals for the optical transmission, a cost-efficient and power-saving transmitter for 50 to 100Gbit/s could be realized. The 2-bit DAC driver with chip dimensions of 1050µm x 750µm integrates PAM-4 encoding circuits with an amplification sub-circuit to drive the co-designed MZM with a power consumption of less than 150mW per EIC.

Integrated prism and microlens array. The prism and MLA from FocusLight are designed for out-of-plane coupling of the InP PIC optical I/O. The prism turns the light beam by 90 degrees for the out-of-plane coupling, and the MLA collimates the expanded beam as shown in Figure 6. The expansion of the beam allows for the relaxation of the alignment tolerances for the fiber array (FA) connector.

The prism and MLA are constructed from silicon. Fabricating the silicon prism for total internal reflection presents a challenge because the KOH solution selectively etches along the (111) crystalline plane, which is angled at 54.7° relative to the standard (100) dicing face. Standard wafers would result in a beam misalignment with the PIC surface, negating the advantages of a surface-normal optical connection. To overcome this, the wafer was specially "mis-cut" to bring the etching plane within 1° of the ideal 45°. Simulations indicate that even a 1° deviation could introduce up to 3dB of optical losses, emphasizing the critical nature of this fabrication process. Additionally, it is crucial to maintain the misalignment between the top and bottom lens features within 1µm relative to each other.

The collimating MLA is produced through the deep reactive ion etch (DRIE) method, which ensures a smooth surface that minimizes light scattering. These microlenses are initially formed on a large wafer and later separated using a dicing saw. Additionally, this surface is precisely positioned to maintain the total optical path length from the PIC facet to the lens top, ensuring effective beam collimation.

For an air gap of 65µm between the PIC facet and the silicon-integrated prism and MLA, the total optical path through the silicon lens measures 550µm, with the wafer itself being 500µm thick. The radius of curvature (ROC) of the collimating surface



is designed to expand the beam in the x-direction to 100µm—achieved with an ROC of 556µm. This beam size was chosen to align with future standardized optical expanded beam connectors. Due to the source's ellipticity, the expanded beam size in the other direction is 128µm, and it remains partially collimated.

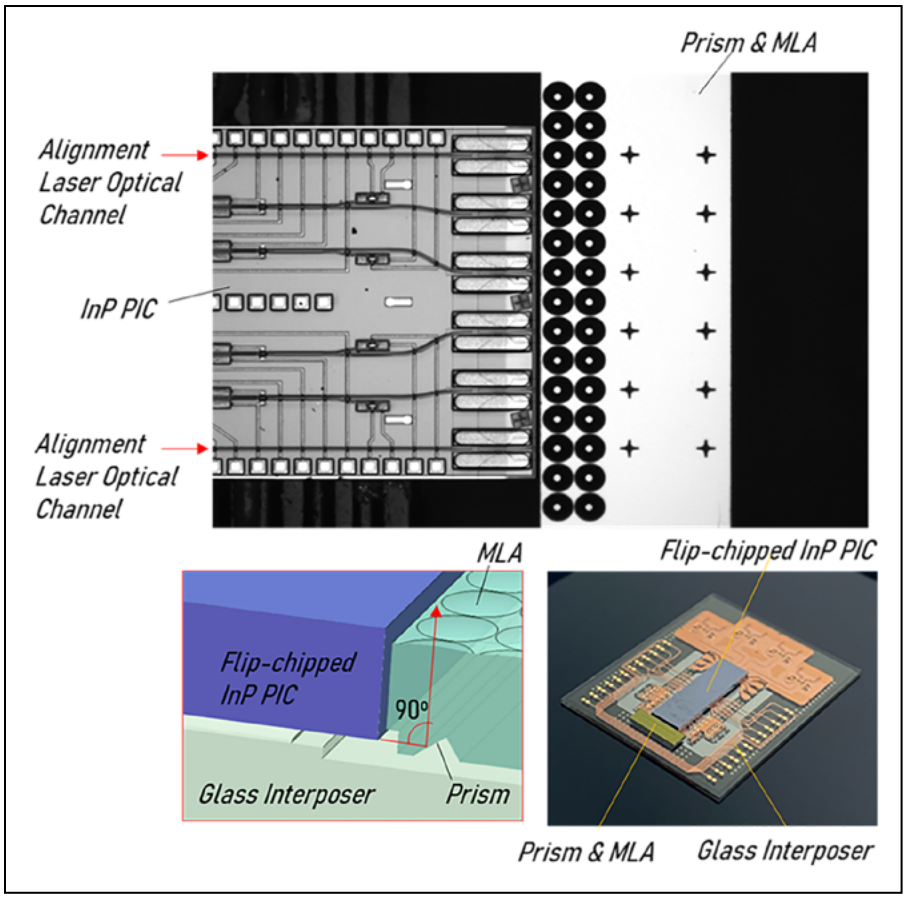


Figure 6: Prism and microlens array actively aligned to an InP PIC for out-of-plane coupling.

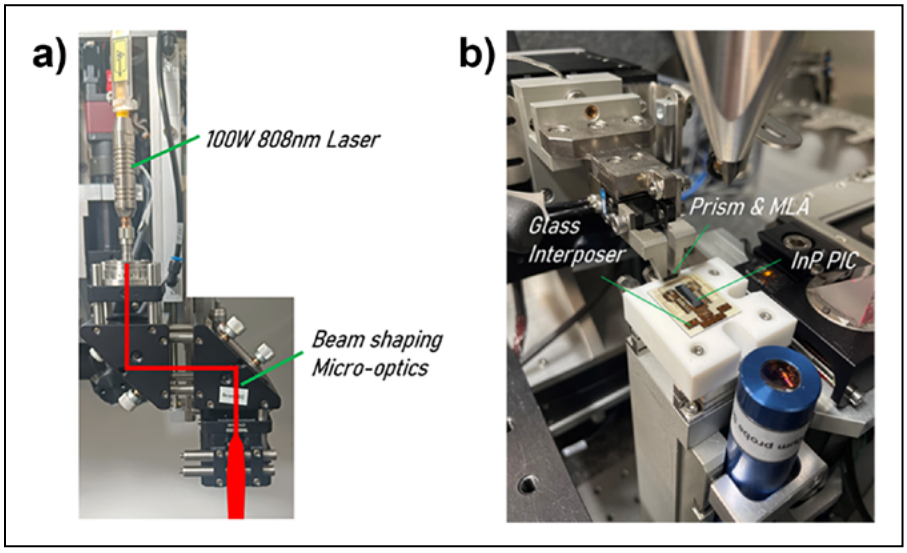


Figure 7: Custom ficonTEC CL1500 for assembly with: a) 100W 808nm laser and beam-shaping optics for flip-chip bonding a PIC to the glass interposer; and b) Active and automated optical setup for the prism and MLA alignment to the PIC.

Packaging assembly process

The CUSTOMLINE and FIBERLINE platforms—from ficonTEC [4]—are developed for the accurate flip-chip, laser-assisted bonding (LAB) of the EICs and PIC and the accurate alignment of the micro-optics on glass interposers, shown in Figure 7. The LAB developed on CL1500 [5] ensures controlled thermal cycles and even heat distribution, thereby enhancing the reliability and performance of components such as laser diodes, photodiodes, micro-optical elements, and lenses. An automated active alignment and attach process of the micro-optics is developed on an F300 platform, where the F300 is tailored for manual or semi-automated MLA pick-ups, closed-loop fast-active alignment, and ultraviolet (UV) epoxy dispensing and curing.

Flip-chip bonding of PIC on glass. A dedicated laser solder reflow system was designed for in-package photonic system integration as shown in Figure 7a. The system utilizes an 808nm laser to bond InP PICs onto glass interposers. Several challenges arose during process development, including handling PICs without obstructing the laser beam, optimizing laser beam shaping, and maintaining precise temperature control. A transparent vacuum pick-up tool (PUT) was developed to apply a uniform downward force during reflow without interfering with the laser.

Micro-optics assembly. Figure 7b shows the setup for active alignment of the flip-chipped PIC to the prism and MLA. The glass interposer was designed so that both the alignment laser diodes of the PIC can be powered up using probe needles, and the prism and MLA placed on top of the glass cavity and actively aligned.

The observed coupling losses range from 1.4 to 1.75dB [6]. These losses can be further reduced through improved mode matching and refinements in the microlens fabrication process. Due to beam collimation, the alignment tolerance of the FA connector increases by approximately 35 times, reaching about 28µm, with a slight discrepancy between beam axes caused by the ellipticity of the couplers.

Summary

We highlighted our ongoing progress in co-packaging flip-chipped EICs and PICs, where the assembled components, as well as the equipment, were simultaneously custom designed. Standardized design rules spawning from this work will contribute to scaling up and lowering cost of photonics

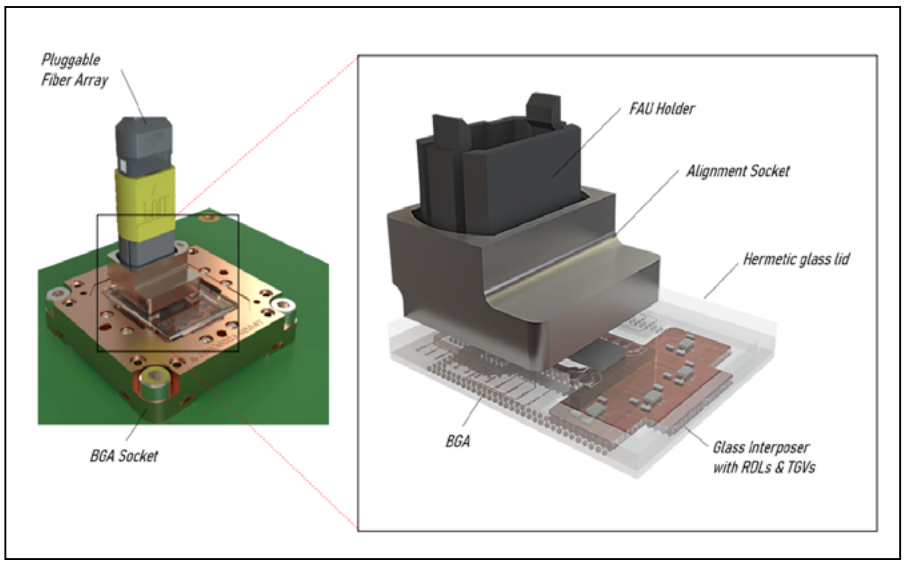


Figure 8: All-glass package with capping lid and socket for a pluggable FA connector, inserted into a BGA socket for an end-user application.

packaging, making it viable for wider industry adoption.

To prepare for the end-user setup, the final package will feature a custom AR-coated capping lid and a 12-channel MPO pluggable fiber connector from SENKO, as illustrated schematically in Figure 8. The all-glass package will be electrically-powered through a JohnsTech BGA socket, designed for a 32 × 40 array of BGA pins with high-frequency spring-loaded probes. A standard BGA bond pad pitch of 0.5mm has been utilized.

The size of the glass interposer has been standardized to accommodate multiple package types with varying applications on the same glass wafer. For example, in addition to the telecommunications package layout discussed here, the same 200mm glass wafer can also include a glass interposer layout for a biomedical application.

TGVs facilitate both direct current (DC) and RF electrical routing to the BGA beneath the interposer. Standardization enables wafer-level handling by testing and assembly equipment, which is essential for scaling up photonics packaging.

Glass interposers are a promising alternative to silicon and organic substrates for high-frequency applications, photonics packaging, and wider adoption in the semiconductor industry. While challenges such as brittleness and process maturity exist, glass technologies are enabling precise micro-structuring, via formation and high-frequency/high-density electrical interconnects making glass-based interposers increasingly viable in advanced photonic packaging solutions.

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Biographies

Prof. Peter O'Brien is head of the Photonics Packaging & Systems Integration Group at the Tyndall Institute, University College Cork, Ireland. Prof. O'Brien previously founded and was CEO of a start-up company manufacturing specialty photonic systems for biomedical applications, which he sold in 2009. Before this, he was a researcher at the California Institute of Technology and at NASA's Jet Propulsion Laboratory, where he was involved in developing sub-millimeter wave devices for remote sensing applications. He received his degree and PhD in Physics from Trinity College Dublin and U. College Cork. Email: peter.obrien@tyndall.ie

Das Kumar is a Senior Researcher at Tyndall National Institute, University College Cork, Ireland. He finished his PhD in EEE from U. of Nottingham, UK and specializes in advanced photonic packaging technologies like glass interposers, for high-speed and high-density electrical and optical interconnects. In his former role, he developed waveguides in glass using ultrafast laser inscription technology. At Tyndall, he manages PhotonicLEAP and leads design of RF packages for photonic applications. Email das.kumar@tyndall.ie

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Impact of BGA solder metallurgy on BLR failure modes in flip-chip packaging

By Jaimal Williamson, Yutaka Suzuki [Texas Instruments]

With the global proliferation of high-computing systems driving trillion operations per second to support advanced driver assistance systems (ADAS) applications, enhancing the semiconductor packaging reliability margin is a quintessential responsibility for packaging engineers. The initiative to establish a continuous-improvement mindset befitting an automotive target of zero defects requires a deep understanding of material science principles that includes the chemical structure and material property relationships of organic packaging materials and the strain-rate-dependent viscoplastic properties of solder materials.

Flip-chip ball grid array (FCBGA) packages are becoming analogous to "servers on wheels," as advanced design rules (i.e., a tighter bump pitch at the first-level interconnect, finer substrate lines and spaces, higher power densities) continue to be trends necessitating high-density interconnect routing. **Figure 1** illustrates a FCBGA package supporting a myriad of high-end applications. As a result, chip-to-package interaction becomes more challenging, as the implementation of advanced design rules drives specific packaging features such as a reduced cross-sectional area of copper lines, a thinner substrate core, and a higher degree of warpage, which can be exacerbated under Automotive Electronics Council-Q100 reliability conditions [1]. In this article, we'll discuss a board-level reliability (BLR) study of two common lead (Pb)-free alloys as the BGA solder ball in flip-chip packages. These Pb-free alloys are denoted as alloy A and alloy B. Alloy A is bismuth free, whereas alloy B contains less than 5% bismuth.

Bismuth-contained solders are well-known for having higher fracture toughness, which is expected to show higher mechanical reliability under the temperature cycling test. The fundamental mechanical behavior of bismuth-contained solders is prone to other mechanical failure risks, however. Failure modes include copper (Cu) metal pad and trace cracking, and build-up passivation film cracking. We also discuss the methodologies to assess expected failure modes of two different alloys undergoing reliability tests, using a combination of finite-element-analysis (FEA)-based thermomechanical modeling and empirical test results. FEA-based thermomechanical models reflecting strain-rate dependent viscoplastic material represented by the Anand model, combining the image processing technique, and failure analysis reports, enabled the details to be reflected for a deep understanding of root causes.

Understanding failure modes under dynamic temperature extremes requires a methodical approach to discover the root cause. For example, at the material characterization stage, the packaging engineer should be conscientious when preparing samples for characterization, as fluctuations in geometric dimensions caused by imperfections (nonuniformity, voids) can have detrimental effects. Sample imperfections can affect the accuracy of material property measurements and cause erroneous values during stress modeling simulations. Characterizing granular details, such as each of the materials that make up the composite FCBGA substrate, is prudent because implementing time-dependent deformation and viscoelastic properties of the organic material set are critical for reliable stress-modeling predictions. This methodology is essential to facilitate the best opportunity for predicting the onset of failure and maximum stress.

As packaging designs become more complex, with demand for 2.5D and 3D multi-chip modules increasing, one result is the significant role that warpage plays because out-of-plane displacement can become a dominant influence to failure modes caused by tensile stresses. Modulus and coefficient of thermal expansion (CTE) are two thermomechanical factors used to decide the bill-of-materials for flip-chip packaging reliability. Because of the anisotropic behavior [2] of certain polymeric materials in the composite substrate, CTE can vary two to three times in the z-direction compared to the

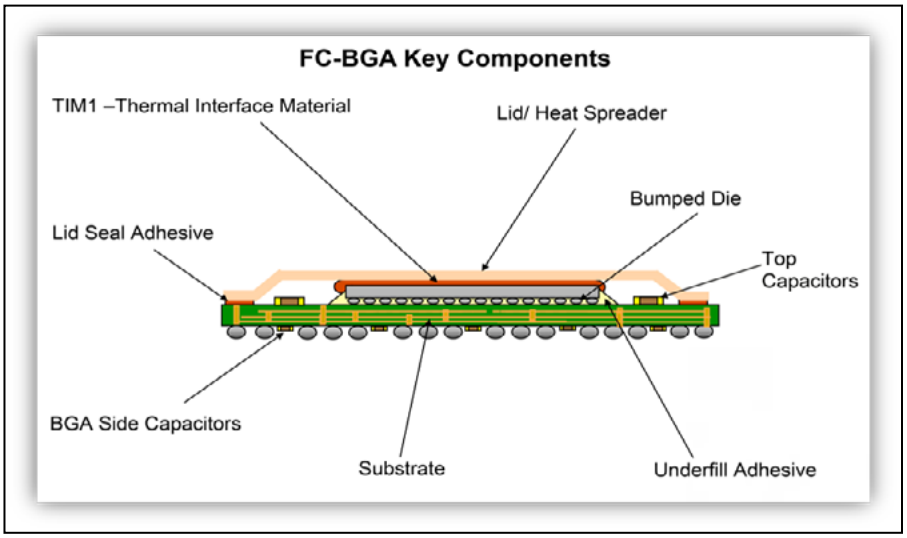
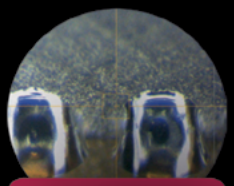


Figure 1: Representative FCBGA package.

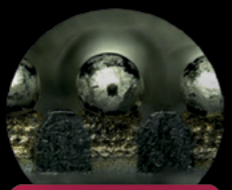
BALL PLACEMENT & LASER SOLDERING

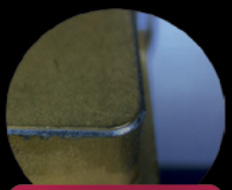

3D-Soldering

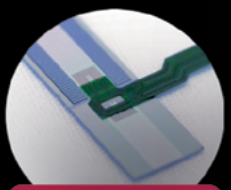

Solder Stacking


Wire Soldering


BGA Soldering


Pre-Soldering of SMD Connector Elements


Lid Sealing for Connectors & IR-Sensors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Through Hole Soldering

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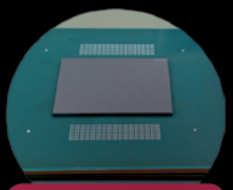
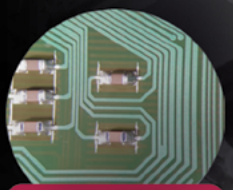

CPU on Interposer Assembly

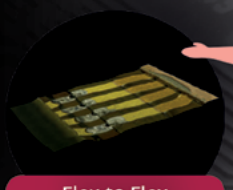

SMD Capacitor Assembly

SOLDER & CHIP REPAIR


BGA Rework


Interconnects of Camera Module


BGA Package Assembly onto Substrate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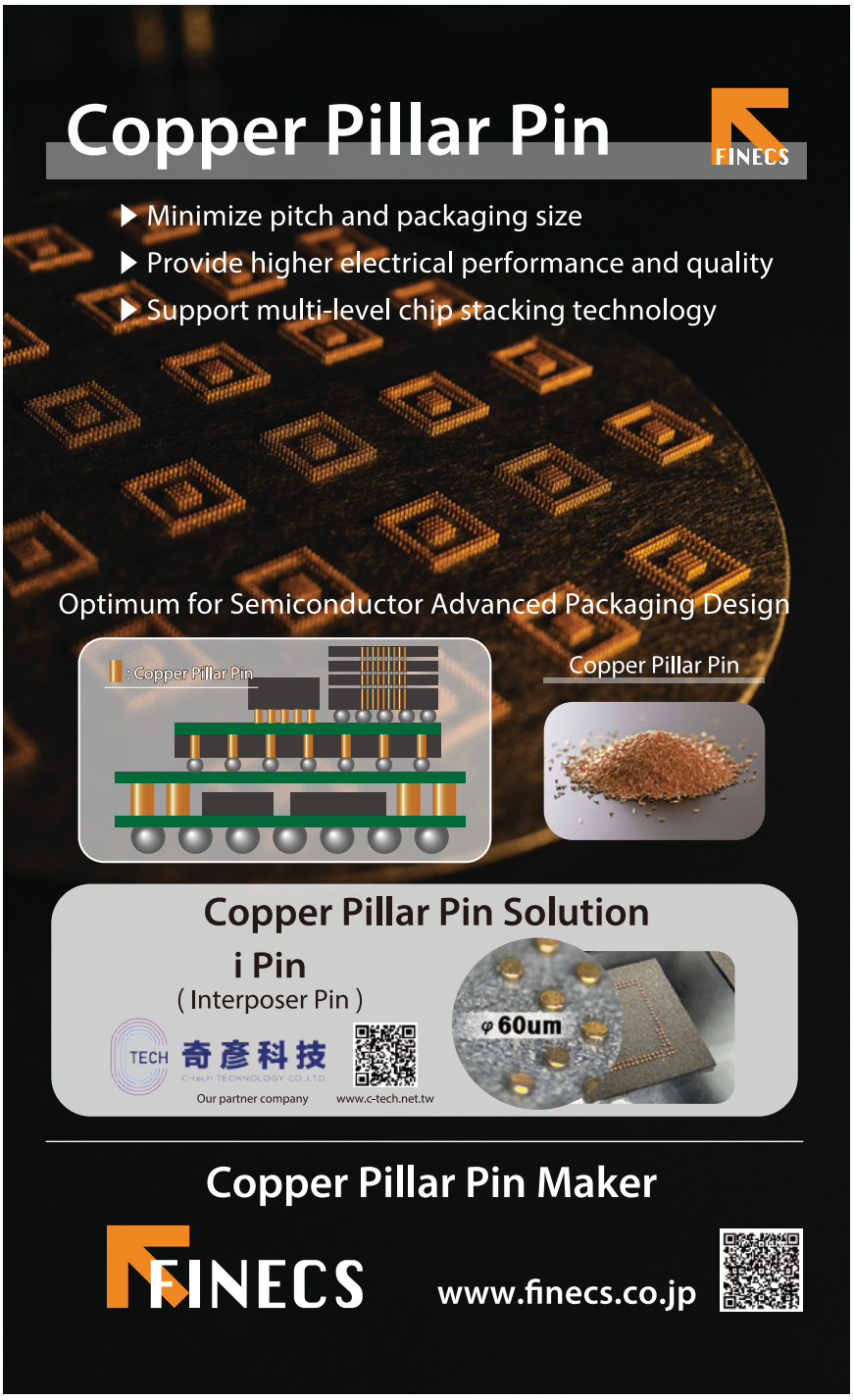
x and y directions. The orientation of polymer chains in the x and y directions can differ significantly in the z direction, which can be compounded by filler or glass reinforcement.

In addition to the considerations above, flip-chip assembly process conditions involving multiple Pb-free reflow temperatures and elevated static heat exposure, such as underfill and lid attach curing conditions, are imperative variables to elucidate the impact of package stresses caused by chemical shrinkage during heating and cooling. As underfill adheres to the die and substrate (as illustrated in Figure 1), understanding the batch-to-batch differences as variations in formulation can affect cure stress as a function of the molecular weight distribution. The bottom line is a holistic approach examining the core fundamentals spanning the characterization of neat and composite substrate materials, assembly processes, and environmental conditions to validate stress modeling against empirical findings.



BLR impact based on BGA alloy material properties

Automotive devices must meet one of the highest reliability standards in the industry. Documenting lessons learned forms a basis for continuous improvements. As such, maximizing BLR findings were studied as a continuous improvement initiative, with a specific focus on studying an alloy with higher modulus and tensile strength. Throughout this article, we will describe the aforementioned alloy as alloy B, and compare it to the incumbent alloy, denoted as alloy A. Table 1 shows a normalized view of the material properties between alloy A and alloy B.

Material property	Alloy A	Alloy B
Young Modulus (GPa)	1	1.45
CTE (ppm / C)	1	0.94
Tensile strength (MPa)	1	3.1
Elongation (%)	1	1.37

Table 1: Normalized view of the material properties between alloy A and alloy B.

The comparison between alloy A and alloy B shows the difference in material properties. Alloy B has an approximately 30% higher modulus and elongation than alloy A. In addition, the tensile strength of alloy B is three times that of alloy A. We hypothesize that this disparity in material properties is the reason that different failure modes manifest during BLR.

During BLR testing, the expected failure mode of the second-level interconnect is bulk solder cracking. Figure 2 illustrates bulk solder cracking

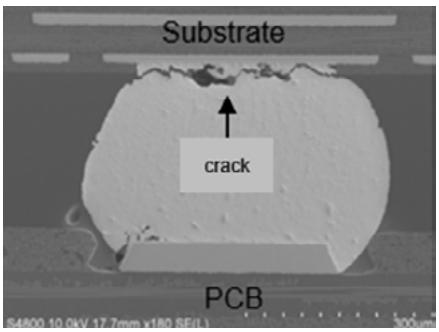


Figure 2: Illustration of bulk solder cracking, with a crack observed on the package side.

Leg	Package type	Body size (mm x mm)	Substrate material set
TV 1	FCBGA	greater than 30mm on a side	HVM material set (ABF as dielectric)
TV 2	FCBGA	greater than 30mm on a side	HVM material set (ABF as dielectric)
TV3	FCCSP	less than 15mm on a side	HVM material set (prepreg as dielectric)
TV4	FCCSP	less than 15mm on a side	HVM material set (prepreg as dielectric)

Table 2: Description of FCCSP and FCBGA packaging types evaluated during BLR.

typically caused by solder fatigue during the temperature cycling test. Temperature cycling conditions (condition G, soak mode 2), as based on Joint Electron Device Engineering Council JESD22-A104 [3], serve as the basis for the hot and cold temperature delta analyzed during stress modeling. Maximizing the cycles to first failure during the condition G temperature cycle is the focus of our continuous improvement initiative.

In this study, we subjected two lidded FCBGA packages (see **Figure 1**) to BLR testing based on JESD22-A104. The only difference was assembling the parts with alloy A and alloy B. In addition, we subjected two overmolded flip-chip chip-scale packages (FCCSPs) to BLR testing, again assembling the devices with alloy A and alloy B. **Figure 3** is a representative image of the FCCSP evaluated during this study. **Table 2** lists the attributes of the FCCSP and FCBGA packages. The first cycles to failure and Weibull analysis (not reported) demonstrated high margin as device requirements were exceeded. However, the failure mode for devices assembled with alloy A and alloy B showed divergent failure mechanisms.

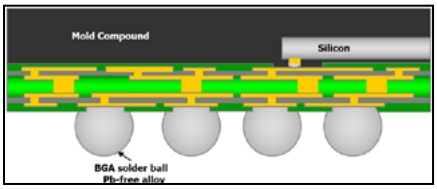


Figure 3: A representative FCCSP.

Hypothesis of failure mode during BLR testing

As stated previously, bulk solder cracking is the preferred failure mode. This failure mode is consistent with the solder fatigue of alloy A, as illustrated in **Figure 2**. In contrast, alloy B exhibited a different failure mode that occurred at the BGA pad – that is not in the bulk solder. With both the FCCSP and FCBGA package types, the BGA Cu pad cracking at the solder mask opening was the onset of failure during BLR testing.

Figure 4 shows an example of the FCCSP failure mode at first cycles to failure, which far exceeded the device requirements. Similarly, the onset of failure for the FCBGA package having a more compliant Ajinomoto buildup film (ABF) dielectric material than the fiber-reinforced prepreg dielectric material used for the FCCSP device, also failed at the BGA Cu pad.

The modulus and CTE of the ABF dielectric are approximately 6 times and 11 times lower, respectively, than the fiber-reinforced prepreg dielectric material. Because of the disparity in material properties, the vector of the crack propagation path between the FCCSP and FCBGA package presented an observable difference. **Figure 5** shows the onset of failure in the FCBGA package as assembled with alloy B.

As previously mentioned, the failure mode between the FCCSP and FCBGA packages exhibited divergent crack propagation paths. Our hypothesis is that the failure mode develops as illustrated in **Figure 6**. Based on **Table 1**, because alloy B shows a higher fracture strain energy than alloy A, the thermal stress in the Cu pad is expected to accumulate without solder cracking under the temperature cycling test. The thermomechanical models shown in **Figure 7** estimate the Cu pad crack risk between the two alloys—assuming that the solder cracking issue does not occur. From the chart, you can see that alloy A has a lower Cu pad crack risk than alloy B after the second cycle. In

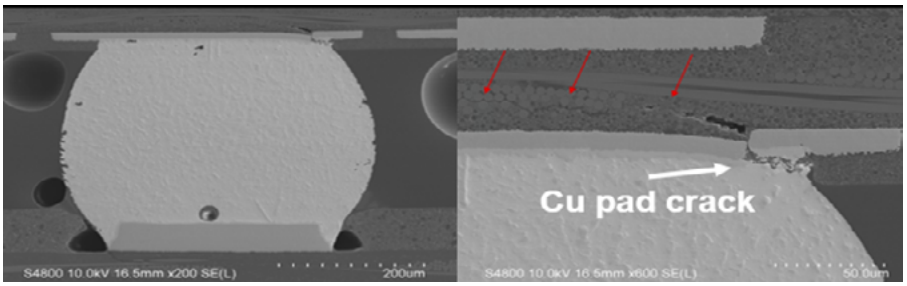


Figure 4: Onset of failure with FCCSP during BLR with alloy B.

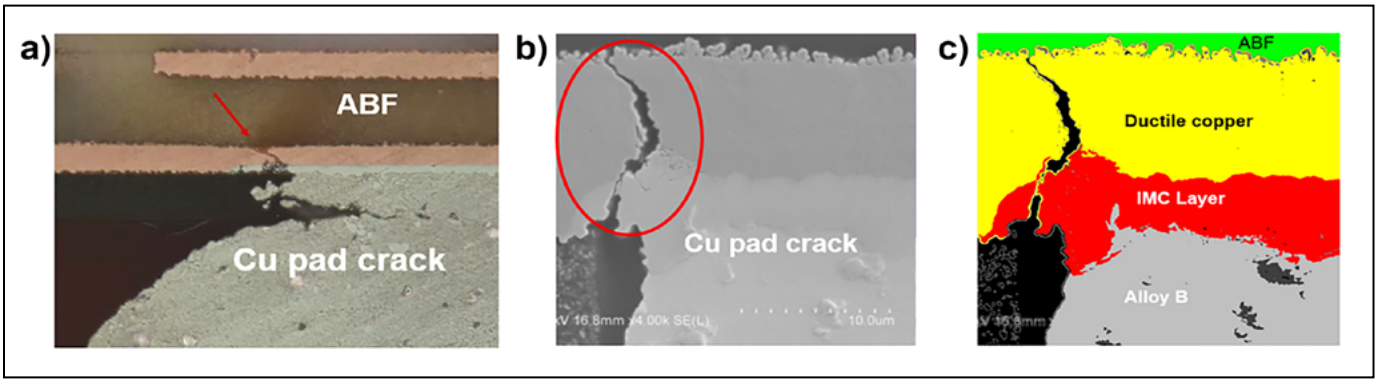


Figure 5: Onset of failure in a FCBGA package during BLR with alloy B: a) A low-magnification optical micrograph; b) A higher magnification scanning electron microscopy image (SEM); and c) Delineation of alloy B, intermetallic compound (IMC) layer, ductile BGA Cu pad and the underlying ABF material.

addition, alloy A is expected to generate bulk solder cracking as a major failure mode given its inherently lower fracture strain energy (lower than alloy B).

As for alloy B, if the accumulated strain energy in the Cu pad exceeds the fracture toughness, a Cu pad crack would occur. This is confirmed from the stress contour map of the Cu pad shown in **Figure 8**. The critical stress point is almost consistent with the actual Cu pad location from the failure analysis. Because the crack propagation rate through the IMC layer is expected to manifest faster than ductile materials, the crack propagated immediately through the IMC layer. The stress concentration region should move to the tip of the crack. **Figure 9** shows the thermomechanical model with stress vector analysis to estimate the crack propagation direction. The critical stress points and propagation direction of the crack using the thermomechanical models are almost consistent with the empirical test result.

In the FCBGA package, the crack propagation vector follows a more upward path, with the crack trajectory traversing the Cu pad and underlying ABF material, and meandering toward the Cu layer above the bottommost Cu layer in the substrate. In contrast, the FCCSP offers a higher degree of rigidity with the fiber-reinforced prepreg in that it drives more of a

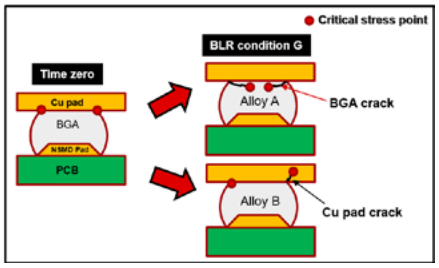


Figure 6: Hypothesis of the failure mode between alloy A and alloy B.

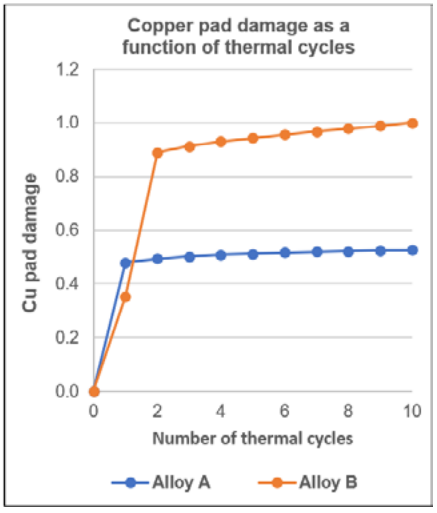


Figure 7: Cu pad damage between alloy A and alloy B as a function of the temperature cycle.

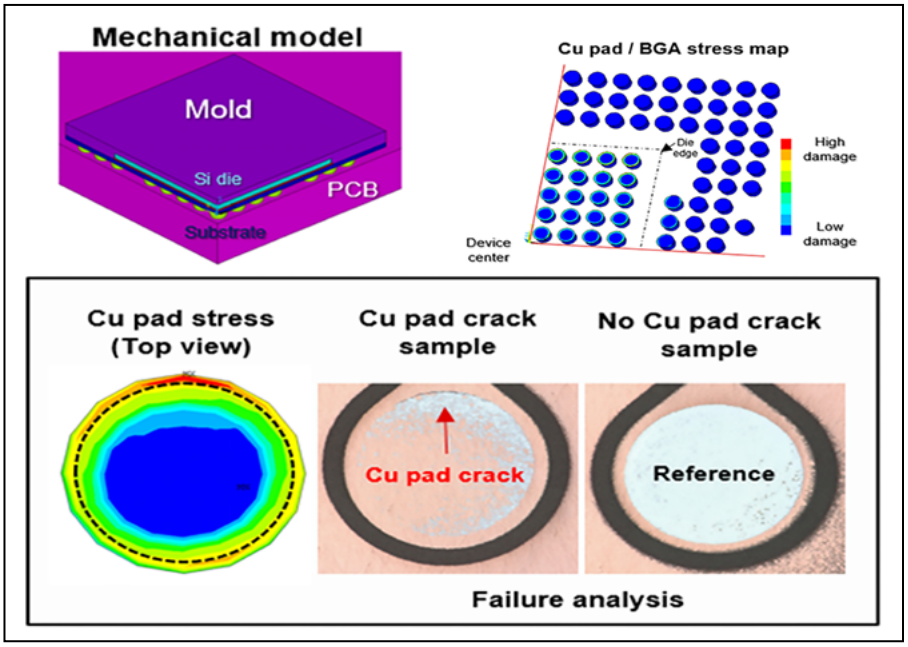


Figure 8: An example of the thermomechanical modeling result for the Cu pad crack risk.

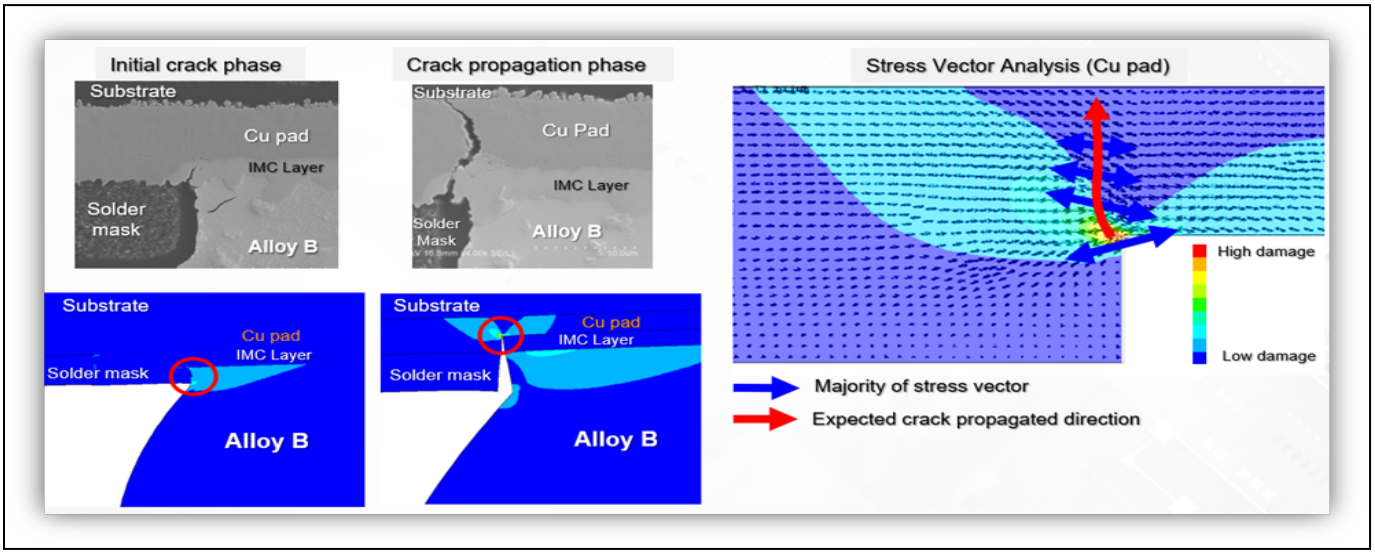


Figure 9: Stress contour map of plastic strain energy for the ductile materials: a) Crack initiation phase; b) Crack propagation phase; and c) Stress vector analysis of the Cu pad.

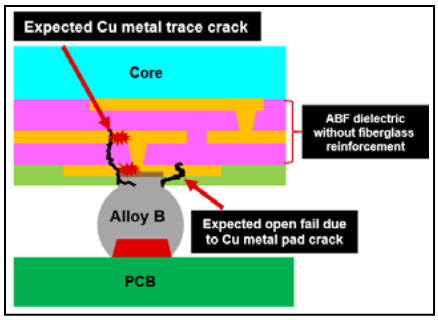


Figure 10: Crack propagation path for the FCBGA package with alloy B.

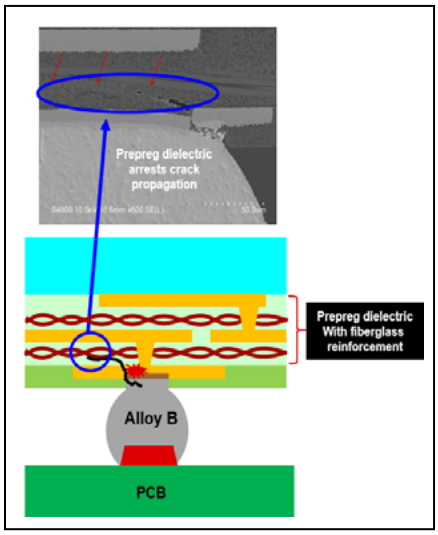


Figure 11: Crack propagation path for FCCSP with alloy B.

meandering crack propagation path laterally throughout the prepreg dielectric material. **Figures 10** and **11** demonstrate the vector of the crack propagation path between the FCBGA package and FCCSP, respectively. As the figures show, the crack propagation path penetrates more in the FCBGA package because of the difference

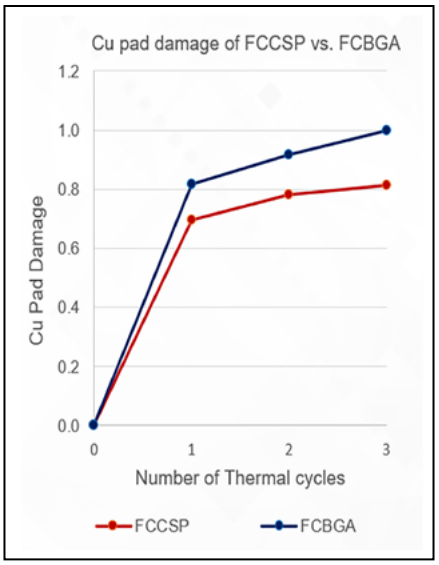


Figure 12: Comparison of Cu pad damage with the FCBGA package and FCCSP.

in material properties between ABF and prepreg dielectric materials. In **Figure 11**, the fiberglass reinforcement provides a means to arrest the crack propagation. **Figure 12** compares the Cu pad damage between the FCCSP and FCBGA package.

Summary

Instilling materials science and engineering principles to establish a fundamental approach to understanding flip-chip packaging failures is a cornerstone to problem solving. We used an FEA-based thermomechanical modeling approach to study the varying failure mechanisms during BLR testing of FCCSP and FCBGA packages assembled with two different Pb-free alloys. The output of BLR testing compared the performance of both flip-chip packaging types assembled with alloy B, which had a higher tensile strength and modulus than alloy A. Alloy B initiated a crack propagation failure mode emanating at the BGA Cu pad during BLR testing.

Thermomechanical models of the critical stress points and crack propagated direction were consistent with empirical test results as validated by failure analysis. The material composition of the dielectric material used in the FCCSP and FCBGA packages played a significant role in the magnitude of the crack propagation vector. A higher degree of damage at the Cu pad was found in the FCBGA package (compared to FCCSP) because the ABF-based dielectric without fiberglass reinforcement limited arrest of the crack propagation.

The synergistic use of FEA stress modeling coupled with best failure analysis practices to corroborate failure modes and crack propagation paths helped drive a continuous improvement mentality for the optimal selection of packaging materials. This is paramount to establishing a zero-defect mindset for automotive devices.

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Biographies

Jaimal Williamson is a Packaging Engineer and Senior Member Technical Staff within Texas Instruments' Worldwide Semiconductor Packaging group, Dallas, TX. His focal areas as a lead technologist include flip-chip platform development of advanced CMOS Si nodes, qualification, and productization to support multiple automotive, industrial, aerospace, and defense applications. He has authored and co-authored 30+ journal articles, conference papers, and technical magazine articles, as well as 25+ U.S. patents in the field of semiconductor packaging. He received a BS in Chemistry from Grambling State U. and a MS in Polymers (via School of Materials Science and Engineering) from the Georgia Institute of Technology. Email: jaimal.williamson@gmail.com

Yutaka Suzuki is a Packaging Engineer and Member Group Technical Staff within Texas Instruments' Worldwide Semiconductor Packaging group, Dallas, TX. He specializes in leading the mitigation of mechanical reliability for advanced IC packaging and systems and in developing Multiphysics system co-design simulation and modeling methodology. He has published over 20 papers and technical magazine articles as an author and co-author in peer-reviewed IEEE conferences and JSME. He is an IEEE and IEEE EPS Dallas Chapter member (Region 5).

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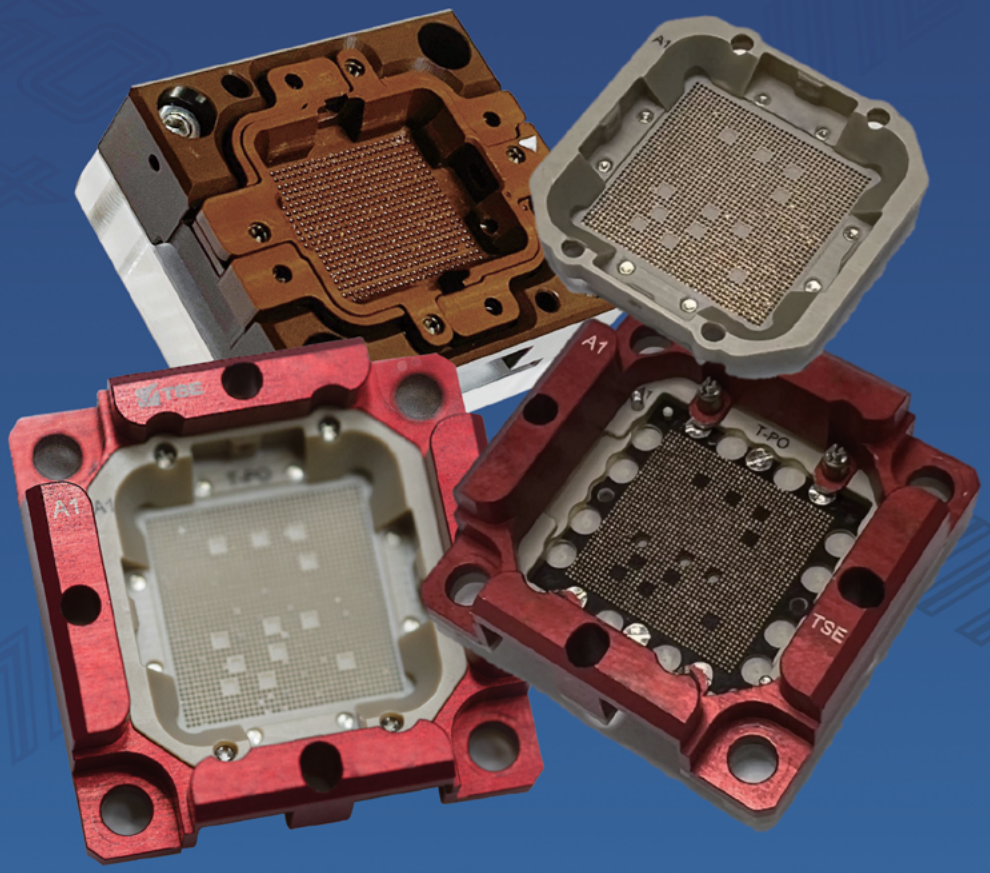

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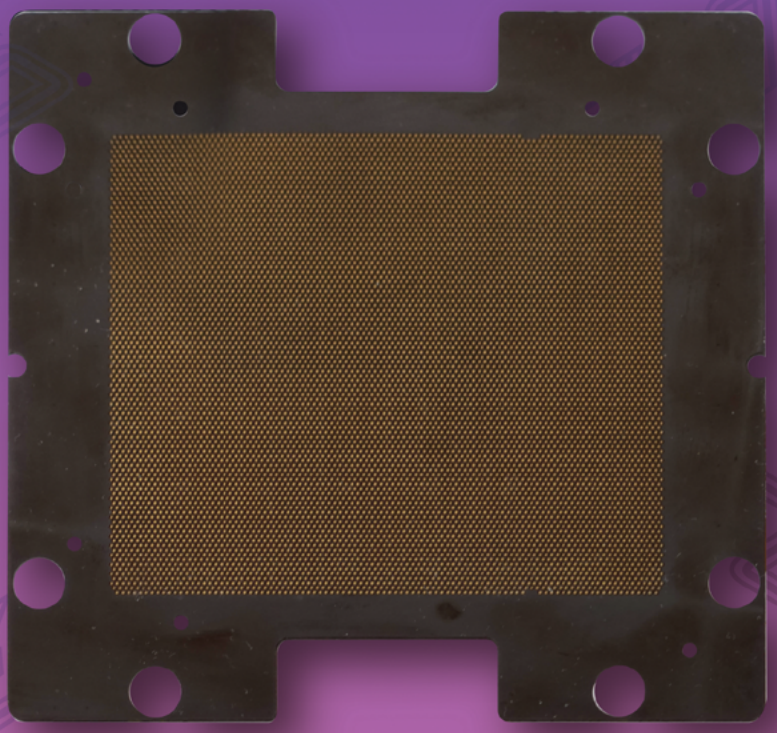

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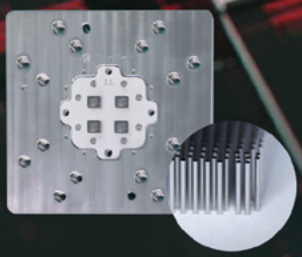

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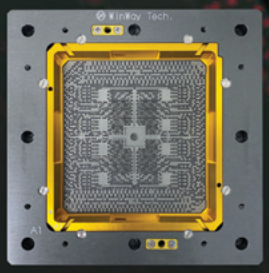

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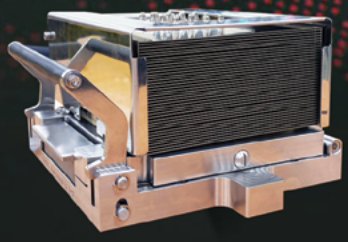

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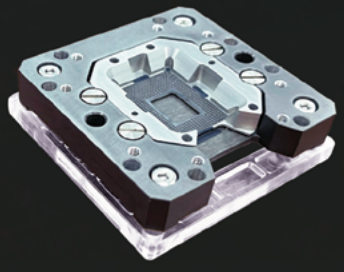
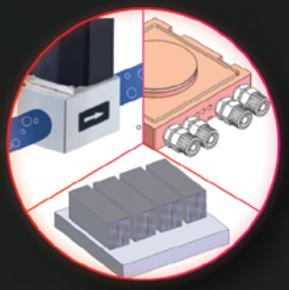


Optical Socket

SerDes 224Gbps PAM4
Optical alignment



Thermal Product

2000W cooling capacity
Temperature : 20 to 150°C

Reliability challenge of underfills in large-size heterogeneous integration FO-MCM packaging

By Liang-Yih Hung, Chia-Wei Chang, Wen-Yu Teng, Andrew Kang, Yu-Po Wang [Siliconware Precision Industries Co., Ltd]

Fan-out multi-chip module (FO-MCM) technology has made it possible to integrate a significant quantity of chips and high-bandwidth memory (HBM) devices into a single package with excellent signal and power integrity. These modules address the market drivers of improved computing performance, memory capacity and bandwidth. However, FO-MCM reliability performance is impacted by the increase in bending stress caused by increased warpage as a result of the much larger package size.

Though underfill material is rather conventional, it plays an important role in a large FO-MCM package. Underfill is a composite material that mainly comprises epoxy polymer and silica (SiO_2) and anti-bleeding agents; adhesive promoters and carbon black dyes are often added to its formulation. Usually, the underfill is dispensed through capillary action to fill the gap between the silicon chip/chip module and an organic redistribution layer (RDL) interposer/substrate to offer physical protection of µbumps/C4 bumps, and acts as a buffer to absorb the stress from coefficient of thermal expansion (CTE) mismatching between the silicon die/chip module and their own carriers.

In this article, the mechanical property and stress strength of a heterogeneous integration fan-out multi-chip module (HI-FOMCM) are investigated. The test vehicle comprises one HI-FOMCM, which is bonded onto an organic substrate. The floor plan of the HI-FOMCM device contained one silicon chip and four HBMs. We used a thermal mechanical analyzer (TMA) and a dynamic mechanical analyzer (DMA) to study the underfill and provide the parameters needed for the models used in the finite element analysis (FEA). The purpose of the FEA is to simulate effects of the glass transition temperature (Tg) and the CTE of the applied underfill on both the warpage of the HI-FOMCM and the corresponding bending stress on the HBM chip. Design of experiments (DoEs) were planned with the studied underfill and validated for MSL3, unbiased highly-accelerated stress testing (uHAST), temperature cycling testing (TCT) and high-temperature storage life (HTSL) testing to discuss the relationship among the reliability results, simulation data, and material properties of the underfills. Moreover, stress-strain curves of the underfill were measured and analyzed to determine the key performance metrics of the HI-FOMCM underfill.

Introduction

The global data center and autonomous vehicles markets are experiencing rapid growth, driven by the increasing demand for high-performance computing (HPC) to support artificial intelligence (AI) workloads. The AI market is projected to grow at an annual rate of nearly 30% from 2025 to 2030. Heterogeneous integration has emerged as a pivotal trend in advancing AI applications by integrating multiple components, such as AI accelerators (graphics processing units [GPUs], tensor processing units [TPUs], application-specific integrated circuits [ASICs]), HBMs, and I/O controllers into a single package. This approach enables high interconnect density and reduces power loss. The evolution of SPIL's advanced packaging modules' size is illustrated in **Figure 1**. Compared to

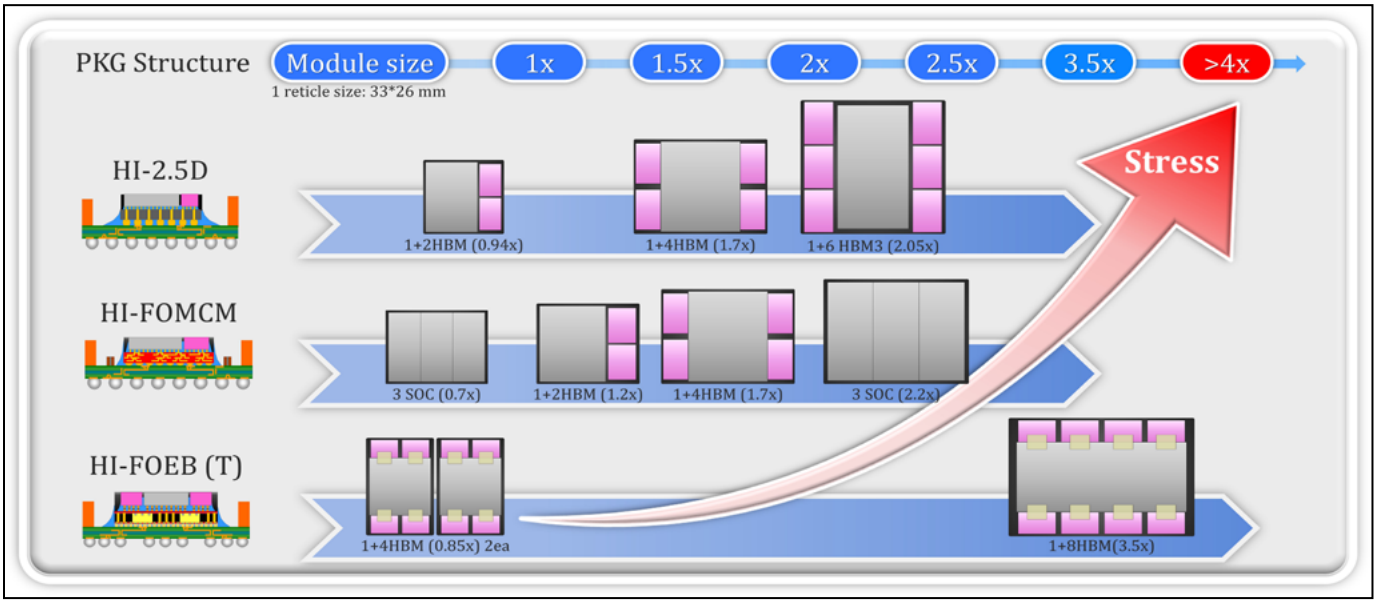


Figure 1: The evolution of the size of advanced packaging modules.

2.5D integration, HI-FOMCMs are more cost-effective, utilizing a RDL instead of a silicon interposer for die-to-die interconnections. However, as the package size increases, thermomechanical stress also rises. For 2.5D integration packages that use a high-stiffness silicon interposer, the bending stress typically occurs at the outer edge of the HBM chip. In contrast, for HI-MCM packages that adopt an organic interposer (RDL), the bending stress is concentrated in the middle region between the ASIC chip and the HBM chip.

HI-FOMCM packages require the use of underfill materials to protect fragile silicon chips (or chip modules) and copper pillar bumps, or solder bumps, while controlling warpage of the package. Figure 2 illustrates two applications of underfill material in HI-

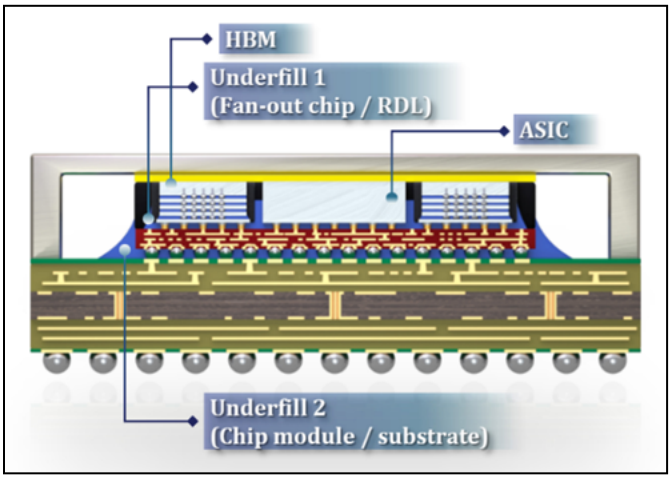


Figure 2: Schematic of a flip-chip-ball grid array with the heterogeneous integration of a fan-out multi-chip module.

FOMCM packages: Underfill 1 is used to fill the gap between the HBM/ASIC and the RDL, while Underfill 2 is used to fill the gap between a chip modulus and substrate in a fan-out multi-chip module. The primary functions of underfill are as follows:

1. To mitigate mismatches in the CTE between silicon chips and their carrier or substrate;
2. To enhance resistance to thermal stress;
3. To protect against physical stress caused by mechanical shocks, drops, and vibrations;
4. To protect against moisture, ionic residues, and unwanted substances; and
5. To promote the adhesion of a component to a carrier or substrate.

However, thermal stress and modulus-related stress between a chip and its RDL on HI-FOMCM packages remain problematic. Therefore, this article shares SPIL's experience in selecting the appropriate Underfill 1 for the HI-FOMCM package.

Evaluation of underfill material

The following sections discuss underfill selection, the HI-FOMCM test vehicle, and the reliability test conditions.

Underfill selection. The material mechanical properties of UF-01, UF-02, and UF-03 are summarized in Table 1. The measurement data were analyzed using an ANSYS static structural module (a three-dimensional (3D) finite element analysis model) to assess stress and warpage. UF-01, a commonly used underfill material in the fabrication of HI-FOMCMs, was validated in this study by applying it as Underfill 1. Simulation results indicated that reducing the material modulus decreases both the warpage and the HBM chip bending stress in the chip module. The simulation results of the warpage and bending stress are shown in Table 2. The chip module containing UF-01 exhibited the highest HBM chip bending stress and warpage at high temperature. Consequently, two underfill materials with lower bending stress than UF-01, namely UF-02 and UF-03, were selected for evaluation. These materials were examined by SPIL Material LAB, which ensured that the fabricated test pieces were identical and

Mechanical properties		Underfill type		
Item	unit	UF-01(POR)	UF-02	UF-03
CTE 1 / 2	ppm/^{0}C	38 / 82	50 / 100	45 / 115
Tg (by DMA)	^{0}C	217	123	169
Modulus RT / HT	Gpa	6.1 / 1.8	5.2 / 0.08	5.4 / 0.4
Adhesion on Chip	Kg	12	21	14
Adhesion on EMC	Kg	15	16	15

Table 1: Underfill mechanical properties.

UF Type		UF-01(POR)	UF-02	UF-03
HBM bending stress	-	1X	0.68X	0.77X
Chip module warpage at RT/HT	µm	286/101	274/77	281/89

Table 2: Simulation results with respect to stress and warpage.

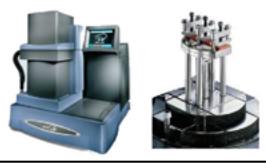
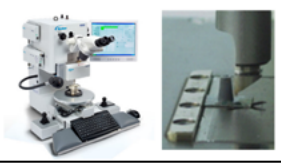
Analysis item	CTE	Modulus	Adhesion	S.S.Curve
Equipment	TMA	DMA	Shear Tester	UTM
Mode	Expansion	Dual cantilever	Pudding shear test	Tensile test
Sample dimension	6.5*6.5*15mm^3	60*10*2mm^3	Dia. * height: 4*3mm^2	ASTM D638 type 1
Temperature	25~260^{0}C	25~260^{0}C	25^{0}C	25^{0}C
Note				

Table 3: Equipment used for underfill property measurements.

that all measurement parameters were consistent to maintain accuracy. The dimensions of the test piece and parameters of the measurement platform are listed in **Table 3**.

The CTEs and storage modulus of the underfill materials were measured using a TMA and DMA, respectively. Adhesion strength between the underfill and chip/epoxy molding compound (EMC) were evaluated using a Dage 4000 Bondtester. The underfill was applied in a pudding mold shape over the surface of the chip/EMC. After curing, the underfill was sheared at a height of 20µm to obtain its adhesion strength. To measure the stress-strain behavior, samples were prepared following ASTM D638 (Type 1 dimensions) and tested using a universal testing machine (UTM).

HI-FOMCM test vehicle. The selected underfill materials were evaluated in a test vehicle comprising a HI-FOMCM. The test vehicle is shown in **Table 4**. The test vehicle contained a 72.5mm × 70mm package that bonded with a 45mm × 30mm HI chip module (1 chip + 4 HBM modules). The fan-out multi-

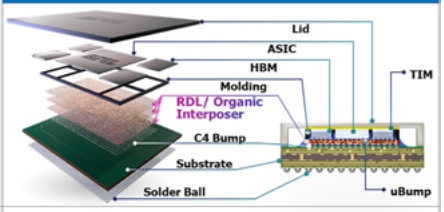
Package Structure		HI-FOMCM (1 Chip + 4 HBM) 
Package size	mm²	72.5 x 70
Chip module size	mm²	45 x 30
ASIC size	mm²	28 x 24
HBM size	mm²	8 x 12 (4 pcs)
RDL Layer	-	3L
Substrate layer	-	18L
Heat sink type	-	Stiffener ring

Table 4: Information on the package selected for evaluation.

chip module was flipped and bonded to the substrate. The HI-FOMCM fabrication process is illustrated in **Figure 3**. We employed a chip-last process, which was initiated by stacking three RDLs on the wafer surface. Subsequently, one chip and four HBM modules were assembled onto the wafer. The space beneath the fan-out chip was then filled with an underfill (Underfill 1); this underfill was later subjected to examination. Next, a liquid molding compound was applied in a compression molding process to protect the chip module, which was then combined with a substrate, and another underfill (Underfill 2) was used to fill the space between the chip module and substrate. Additional steps were then performed to complete the fabrication of the HI-FOMCM.

Reliability test condition. This study also conducted several experiments to evaluate the performance of selected underfill materials. The testing conditions were as follows: JEDEC Level 3 preconditioning (moisture sensitivity level of 3, 30°C with a relative humidity of 60% for 192 hours) with three reflows at 245°C; 700 cycles of (TCT) under condition B (−55 to 125°C); 96 hours of uHAST at 130°C with a relative humidity of 85% after preconditioning; and 1000 hours of HTSL at 150°C. After the aforementioned reliability tests, scanning electron microscopy

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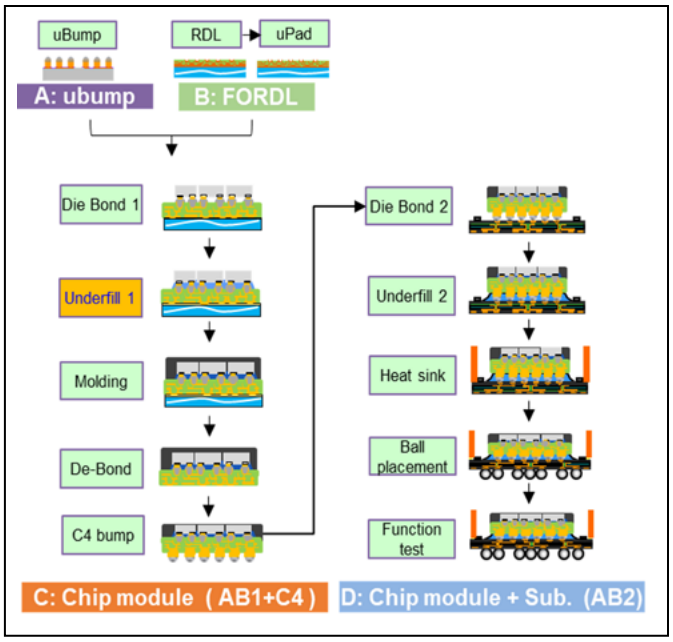

Figure 3: HI-FOMCM fabrication process.

(SEM) was employed to examine the cross section of the HI-FOMCM for any structural damage caused by bending stress.

Underfill materials verification results

SEM images of the cross sections of the chip modules subjected to MSL3 tests containing UF-01, UF-02 and UF-03 are presented in **Figure 4**. The SEM images of UF-01 revealed cracks originating from the bottom underfill region

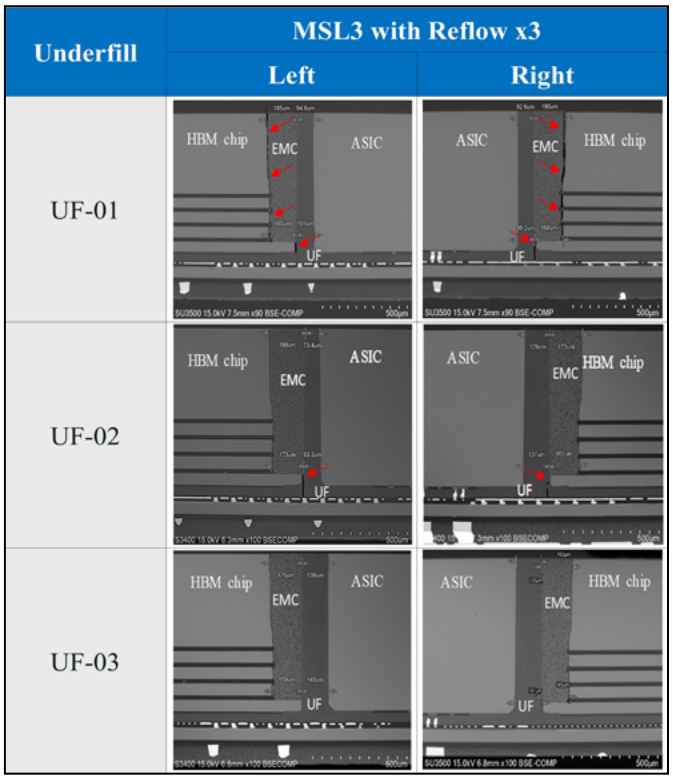

Figure 4: SEM image of a cross section after the MSL3 test.

and propagating to the sides and top of the HBM chip. To investigate the root cause of these cracks, an ANSYS 3D finite element analysis was conducted. The stress contour simulations revealed that the maximum stress points were concentrated at the corner of the HBM chip, as illustrated in **Figure 5**.

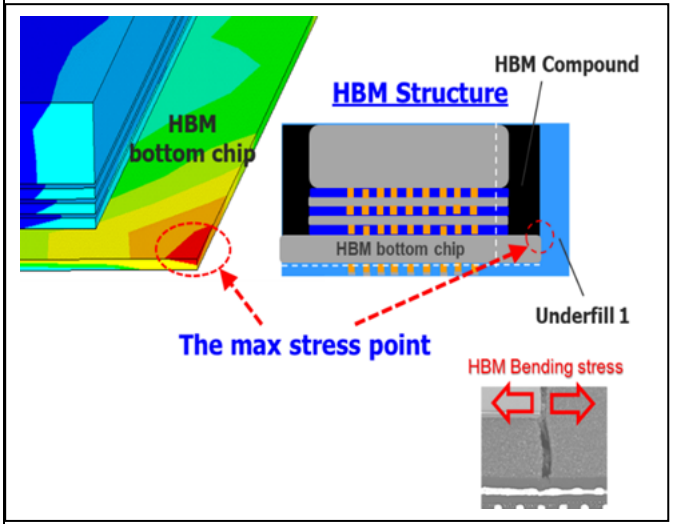

Figure 5: Contour of a weak point at a corner of a HBM chip.

SEM images of UF-02 shows the cracks in the chip module extended only from the corner of the HBM chip toward the bottom underfill area—the cracks did not extend upward to the sides and top of the HBM chip. This confirms that reducing HBM chip bending stress and chip module warpage can effectively mitigate crack formation. However, experimental results presented some unexpected findings. Although UF-02 exhibited the lowest bending stress and chip module warpage, cracks were still observed in its chip module. On the other hand, no cracks were observed in the chip module containing UF-03, suggesting that other factors beyond bending stress and warpage play a role in crack formation.

The stress–strain characteristics of the underfill materials are shown in **Figure 6**. The calculated areas under the stress–strain curve for UF-01, UF-02, and UF-03 were 65, 177, and 250mm^2, respectively. A large area under the curve reflects higher ductility and elongation. Whereas a smaller area indicates brittleness and increased fracture risk. Based on this, UF-03,

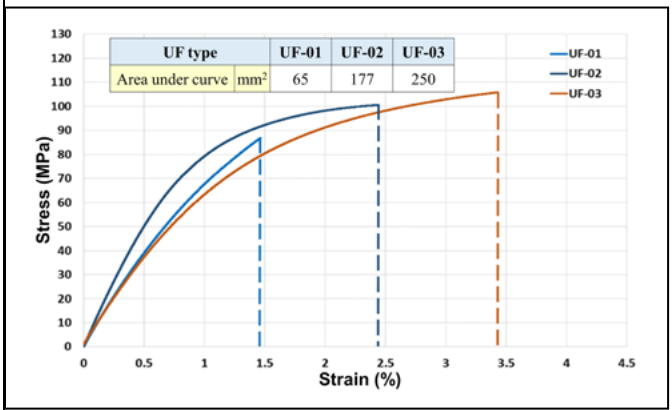

Figure 6: Stress–strain curves of selected underfill.

which exhibited the largest area under the curve, demonstrated the best suitability as an underfill material for HI-FOMCM applications. From the perspective of material properties, UF-02 was initially expected to exhibit higher ductility and elongation than UF-03 due to its lower Tg and modulus. However, contrary to expectations, the experimental results revealed the opposite. Further analysis showed that UF-03 was mixed with flexibilizers, enhancing its inherent elasticity and significantly improving its ductility and elongation. This improvement reduced internal stress within the material and prevented crack formation, as illustrated in **Figure 7**.

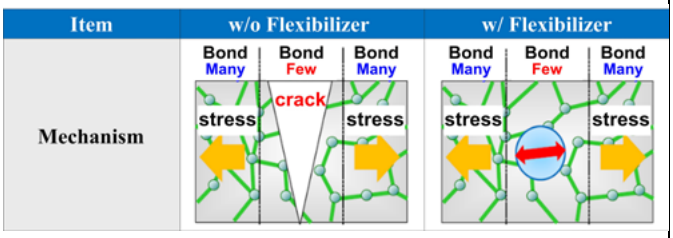

Figure 7: Crack mechanism by stress with and without a flexibilizer.

To ensure the reliability of UF-03, SEM cross sections of the chip modules containing UF-03 were analyzed after various reliability tests, including MSL3 + uHAST (96h), MSL3 + TCT (700 cycles), and HTSL (1000h). The results, shown in **Figure 8**, indicated no cracks were observed under these conditions. These findings confirm that chip modules

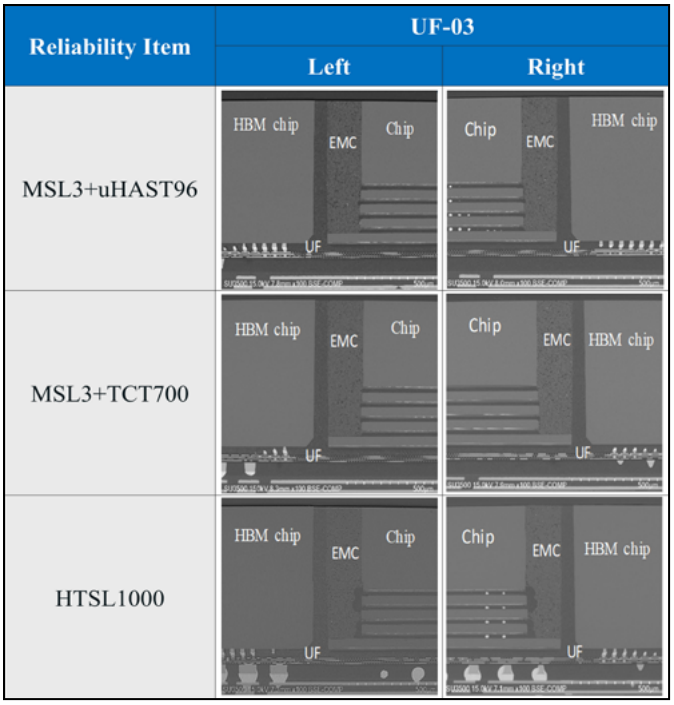

Figure 8: Cross section of UF-03 as observed using a SEM after the reliability assessment.

with UF-03 can pass all reliability tests, making it a suitable underfill material for high-performance chip modules.

The findings of this study emphasize the importance of selecting underfill materials not only based on mechanical stress reduction, but also on intrinsic material properties, such as ductility and elasticity. The incorporation of flexibilizers in UF-03 demonstrated the potential of enhancing material performance by modifying its composition. This suggests that future material designs could focus on tailored formulations to meet the specific demands of high-density semiconductor packages.

Summary

This study investigated the mechanical performance and reliability of three underfill materials (UF-01, UF-02, and UF-03) for packaging of HI-FOMCMs. Key findings from the research are as follows:

1. UF-01: Despite its high modulus and use in current applications, UF-01 exhibited cracks originating from the underfill area at the bottom of the HBM chip during MSL3 reliability testing. These cracks extended to the sides and top of the chip, indicating insufficient flexibility and ductility to withstand thermal and mechanical stresses.
2. UF-02: Although UF-02 exhibited the lowest warpage and bending stress, cracks were still observed during reliability tests. This finding highlights that factors beyond warpage and stress, such as material ductility and elongation, significantly impact crack prevention.
3. UF-03: UF-03 demonstrated superior performance, passing all reliability tests, including MSL3, uHAST, TCT, and HTSL, without forming cracks. The inclusion of flexibilizers in its formulation enhanced its ductility and elongation, reducing stress and preventing crack formation.

These results emphasize the importance of selecting underfill materials with low modulus and high ductility for use in HI-FOMCMs. Materials like UF-03 that exhibit a larger area under the stress-strain curve provide greater resistance to stress-induced damage.

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Biographies

Liang-Yih (Joe) Hung is a Department Manager of Corporate R&D at Siliconware Precision Industries Co., Ltd., Taichung, Taiwan, R.O.C. He received a Masters Degree from the Department of Materials Science & Engineering at National Chung Hsing U., Taiwan. He joined SPIL in 2002 and is in charge of new material development for advanced packaging applications; Email joe65@SPIL.com.tw

Chia-Wei Chang is a Senior Engineer in Corporate R&D at Siliconware Precision Industries Co., Ltd., Taichung, Taiwan, R.O.C. He received a Masters Degree from the Department of Chemistry National Sun Yat-Sen U., Taiwan. He joined SPIL in 2024 and is in charge of new material development for advanced packaging applications.

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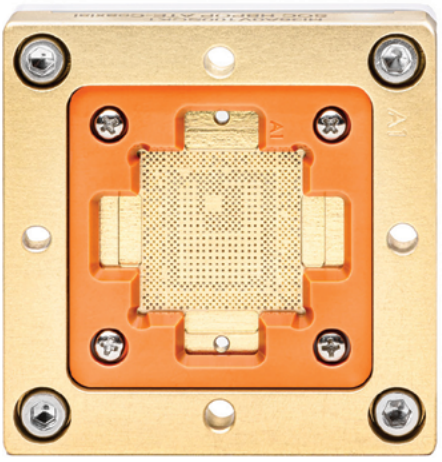

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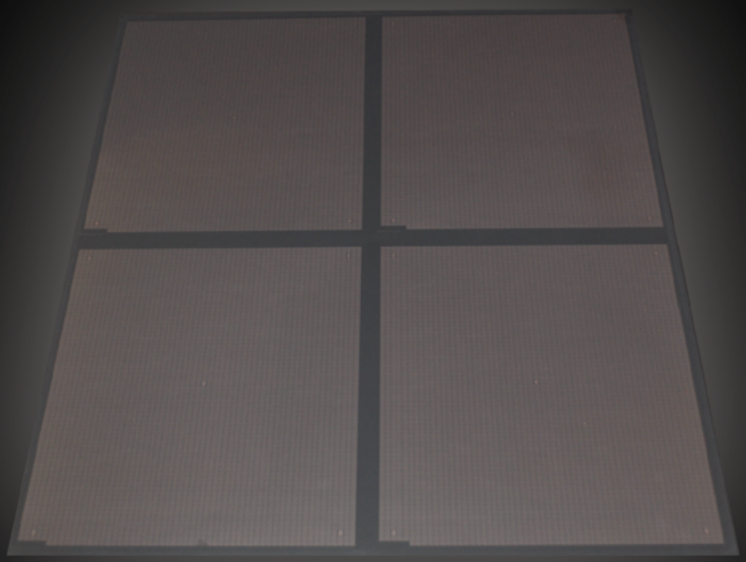
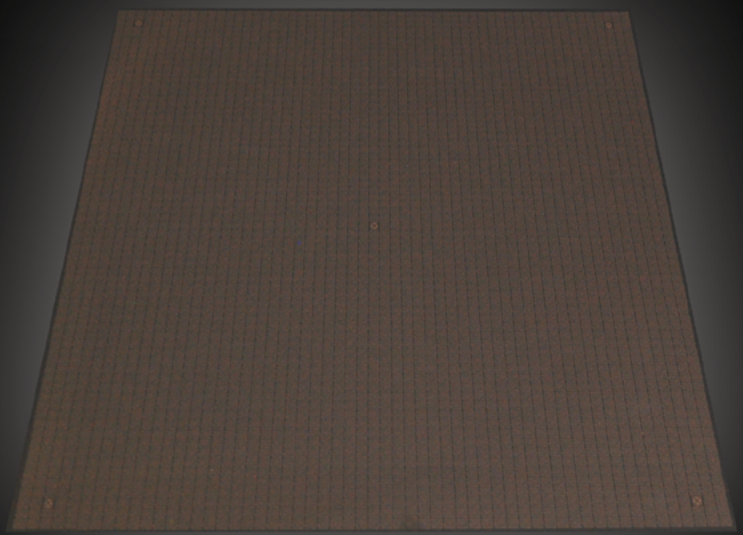


Initial format for 300mm test

designed to utilize existing industry
300 mm probe capacity



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New package solutions for automotive optical sensors

By Weilung Lu, Adrian Arcedera, WonBae Bang, KiDong Sim [Amkor Technology, Inc.]

Automotive optical sensors, including cameras, image sensors, and light detection and ranging (LiDAR) components, are fundamental to the operation of advanced driver assistance systems (ADAS). These sensors play a crucial role in detecting and interpreting the vehicle's surroundings, supplying high-precision data necessary for ADAS functionality. With the evolution of autonomous driving technology, particularly the transition from the Society of Automotive Engineers (SAE) SAE J3016 Level 2 autonomy to Levels 4 and 5, the number of cameras and optical sensors integrated into each vehicle is expected to rise substantially. Industry projections, including those from SAE, suggest that future vehicles could be equipped with 8 to 10 or more cameras per unit.

The widespread adoption of ADAS by automotive manufacturers has significantly enhanced driving safety. These systems provide real-time assistance to drivers, reducing the likelihood of accidents and improving overall road safety. Key ADAS features include adaptive cruise control, lane departure warning, and automatic emergency braking, which have become standard in modern vehicles. As the industry progresses towards increased vehicle automation, the integration of ADAS technologies is accelerating, driving rapid advancements in sensor technology.

Beyond conventional camera-based applications, a range of innovative optical sensor technologies is emerging, further augmenting vehicle performance, safety, and user experience. For instance, ambient light sensors are increasingly integrated into vehicle systems to enhance both safety and comfort. These sensors adjust in-car lighting—including dashboard and console illumination—by detecting external light intensity, thereby improving visibility. They also regulate headlight activation in response to surrounding light conditions, ensuring optimal illumination in low-light environments. With ADAS requiring precise visual feedback, ambient light sensors contribute to a more adaptive, efficient, and user-friendly in-cabin experience.

This article introduces the development of a new optical ball grid array (OBGA) packaging platform designed for automotive applications, with a focus on platform development and compliance with the Automotive Electronics Council (AEC) AEC-Q100 Grade 2 reliability standard. The proposed packaging solution extends beyond traditional cavity OBGA packages, which have been primarily utilized for microelectromechanical systems (MEMS) and sensor applications as illustrated in **Figure 1**.

The cavity OBGA platform, depicted in **Figure 2**, represents a well-established and mature technology that is currently in production for consumer electronics. The introduction of this new OBGA package marks a strategic expansion into automotive optical sensors. This initiative strengthens the company's competitive edge by aligning with the increasing

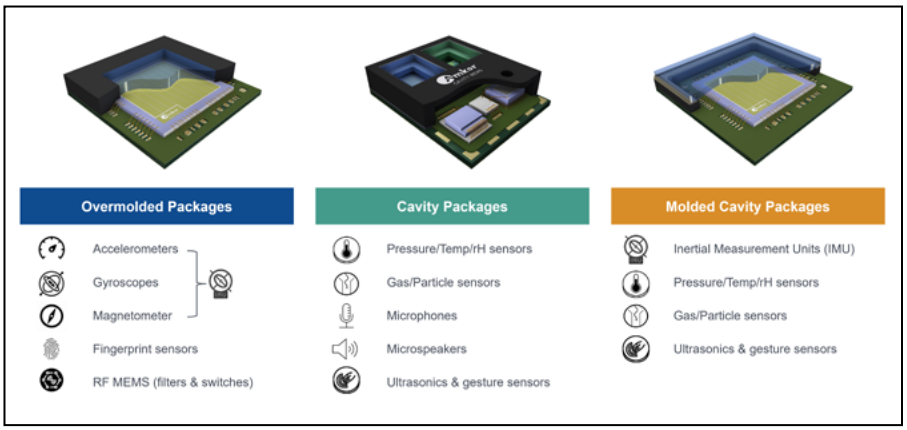


Figure 1: MEMS and sensor packages and applications.

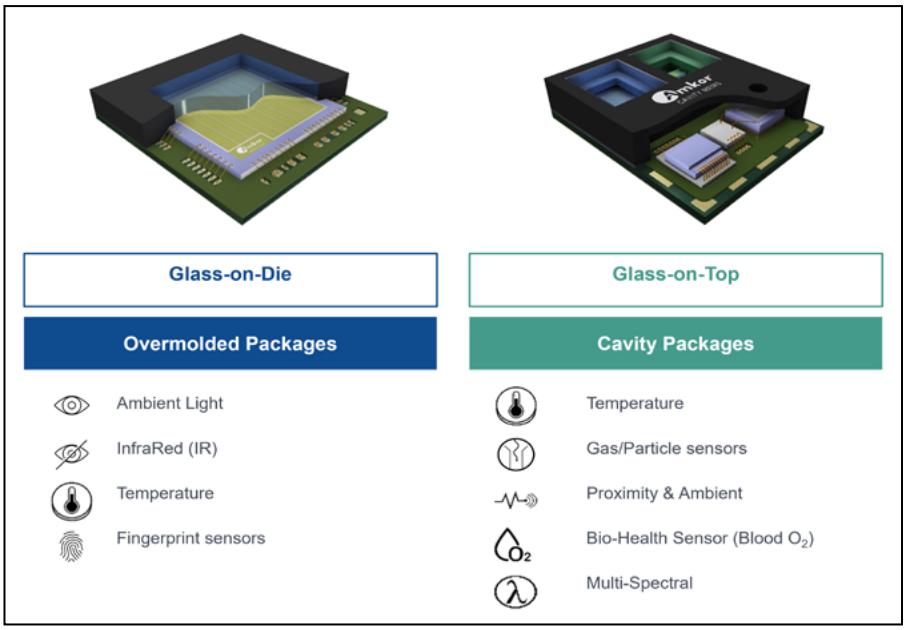


Figure 2: Imaging, optical MEMS and sensing packages and applications.

demand for advanced sensor integration in modern vehicles.

The new OBGA packaging aims to expand the current portfolio by enhancing performance and reliability. Two key technological advancements drive innovation in this packaging platform. The first involves the adoption of glass-on-sensor (GoS) technology, which facilitates the evaluation of clear die attach film (DAF) transmittance while ensuring automotive-grade reliability. This approach enables the package structure to meet the stringent performance and durability requirements demanded by the automotive sector. The second advancement introduces the glass-on-mold (GoM) design, replacing traditional metal or liquid crystal polymer (LCP) lids commonly used in MEMS packaging. This modification eliminates the need for venting holes, effectively mitigating particle contamination in the sensor region. As a result, the optical sensor's reliability and performance are significantly improved.

Designed specifically for automotive optical sensor products, the new OBGA package has undergone comprehensive feasibility studies and rigorous reliability testing. These assessments confirm its structural robustness and suitability for demanding automotive environments, ensuring that the package can withstand extended operational lifecycles and harsh environmental conditions. To address these challenges, advanced toolbox and open tooling capabilities are leveraged to ensure that design for cost (DFC) and design for manufacturability (DFM) considerations are integrated from the initial stages of product development. Prioritizing manufacturing efficiency and scalability allows the delivery of high-performance optical sensor packaging solutions that meet the evolving requirements of the automotive industry.

New package development

To overcome the challenges associated with existing packaging solutions, the new OBGA package integrates advanced molding and lid placement technologies commonly employed in MEMS cavity products. The proposed OBGA package serves as an alternative solution designed to provide enhanced mechanical robustness, accommodating larger sensor sizes anticipated in next-generation automotive applications.

The new OBGA package leverages extensive expertise in cavity MEMS packaging, combined with a proven track record in managing high-end consumer digital camera product lines. This synergy results in a highly reliable and manufacturing-efficient package that meets the stringent performance and durability requirements of the automotive industry. The integration of these advanced technologies ensures that the package maintains structural integrity and optical performance, even under harsh environmental conditions typical of automotive applications.

Two distinct OBGA package variants are shown in **Figure 3**, each designed to address specific application needs. The first variant, GoS, features a compact footprint and is derived from consumer optical fingerprint sensor (FPS) technology. This solution utilizes an established material set and incorporates film assisted molding (FAM) technology, which has been

successfully implemented in the existing product portfolio. The second variant, GoM, represents a completely new design, developed from the ground up to meet the specific demands of automotive optical sensor applications. This innovative structure offers enhanced performance and greater integration capabilities, ensuring long-term reliability and optimal functionality within ADAS and autonomous vehicle ecosystems.

Glass-on-sensor development

The glass-on-sensor configuration involves laminating a transparent die attach film with glass and directly stacking the glass onto the sensor die. A critical characteristic of this structure is the absence of any gap between the sensor and the DAF, ensuring seamless optical transmission. Given the importance of optical clarity in sensor performance, evaluating the material properties of DAF for optimal transmittance and thermal stability is a crucial step in the development process.

Optical transmittance and thermal durability of DAF materials are essential for optoelectronic applications, including automotive sensors, display technologies, and optical coatings. The development process assessed transparent die attach films used in GoS packaging, with particular emphasis on their transmittance characteristics and long-term stability under thermal stress.

Three candidate materials—Material A, Material B, and Material C—were selected for evaluation. Film thickness and thermal curing conditions were evaluated for their influence on optical performance. Key parameters, including transmittance across the visible light spectrum (400–700nm) and stability after thermal aging, were analyzed. A detailed summary of the material properties and corresponding performance data is presented in Table 1.

Identifying materials capable of maintaining high optical transmittance while withstanding prolonged thermal stress is a critical requirement for applications demanding long-term reliability and performance. To simulate assembly process operating conditions, the selected materials underwent thermal aging at 175°C for 8 hours. This process was designed to assess their ability to sustain optical integrity and performance stability under extended high-temperature exposure.

The experimental procedure began with the lamination of DAF onto glass substrates at 65°C, followed by an initial optical transmittance evaluation within the 400–700nm wavelength range. The materials were then subjected to thermal aging at 175°C for 8 hours and transmittance measurements were conducted again to analyze any degradation or shifts in optical performance after thermal treatment. These tests were performed on materials with two distinct film thicknesses—10µm and 20µm—to assess how thickness variations influence transmittance retention and thermal stability.

Table 2 presents the transmittance results for the different materials across various wavelengths following thermal aging at 175°C for 8 hours. Among the evaluated

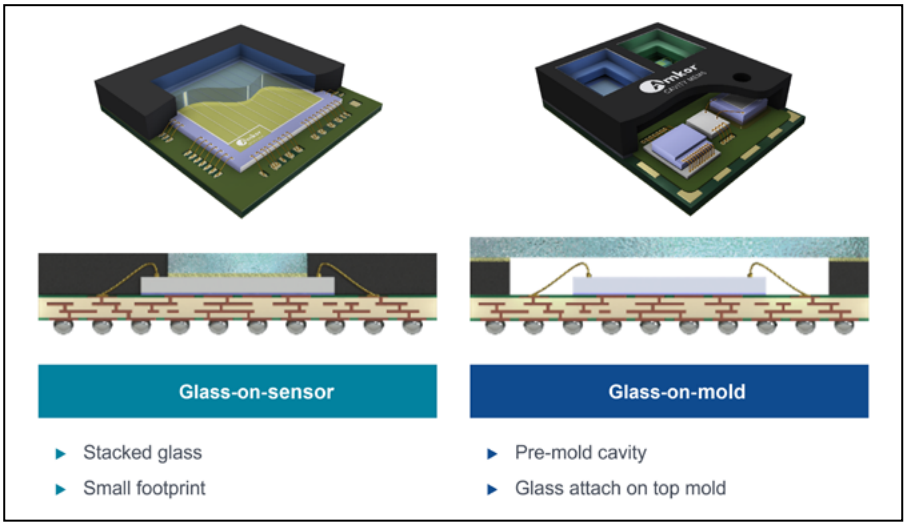


Figure 3: New package structures for automotive optical applications.

Material	Thickness	Tg	CTE	Film Type	Appearance
A	10 µm	41	81	Silica	Transparent (>90%)
B	20 µm	62	75	Silica	Transparent (>90%)
C	20 µm	15	49	Silica	Transparent (>90%)

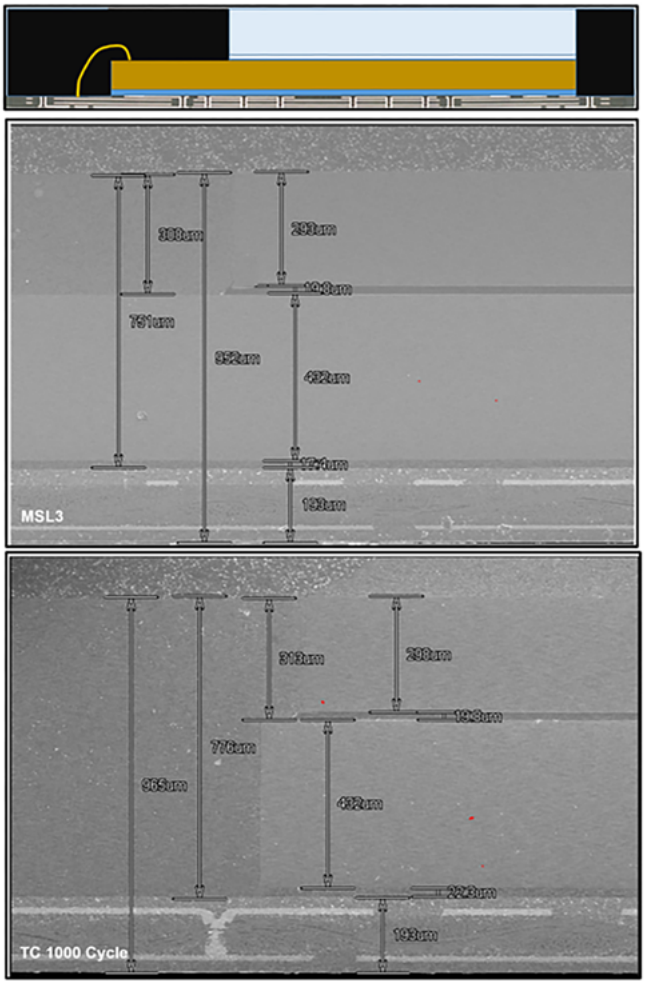
Table 1: Technical property data.

Wavelength (nm)	Material A	Material B	Material C
Red (610–700)	99.99%	99.44%	94.6%
Orange (590–610)	99.71%	99.28%	93.2%
Yellow (570–590)	99.58%	98.28%	92.4%
Green (500–570)	99.45%	97.97%	90.7%
Blue (450–500)	98.45%	95.65%	90.2%
Purple (400–450)	96.34%	91.33%	88.9%

Table 2: Transmittance results after thermal cure at 175°C for 8 hours.

materials, Material A demonstrated superior transmittance across nearly all wavelengths, outperforming the other candidates. Additionally, the results indicate that thinner films (10µm) exhibited higher transmittance compared to thicker films (20µm), confirming the influence of film thickness on optical efficiency.

Both Material A and Material B maintained excellent optical transmittance, consistently exceeding 90% in the 400–700nm wavelength range after undergoing thermal aging. This high retention of transmittance highlights their robust optical stability under extended heat exposure—a critical requirement for automotive optical sensor applications.



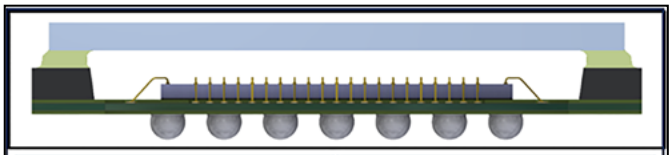
Reliability Results	
MSL 3	12.4 x 8. 6.9 x 7.6 mm
TC (-55~125°C)	500 cycles: Open/Short Passed 1000 cycles: Open/Short Passed
HTS (150°C)	500 hrs: Open/Short Passed 1000 hrs: Open/Short Passed
uHAST (130°C/85%RH)	96 hrs: Open/Short Passed 168 hrs: Open/Short Passed

Figure 4: Reliability results for a GoS package.

Package	Glass-on-Sensor OBGA Test Vehicle
Body Size	12.4 x 8.8 mm
Mold Cap	Film Assist Mold
Die Thickness	Sensor: 425 µm Glass: 300 µm
Film Type	Standard & Material B
EMC Type	Standard
Wire Type	18 µm (0.7 mil) Au
PCB Thickness	2 Layers/0.19 mm

Table 3: Package configuration for the GoS OBGA test vehicle.

Following the material selection process, Material B was chosen for further development due to its balance of high transmittance, thermal stability, and process workability. As detailed in **Table 3**, the next phase involves assembly process optimization and verification of AEC-Q100 Grade 2 reliability, ensuring its suitability for automotive qualification while



Package	GoM OBGA Test Vehicle
Body Size	12.4 x 8. 6.9 x 7.6 mm
Mold Cap	Transfer Mold
Die Thickness	Senser: 200 µm Glass: 400 µm
Die Adhesive	Standard
EMC Type	OMC-2
Wire Type	25 µm (1.0 mil) Au
PCB Thickness	4 Layers/0.6 mm
Reliability Results	
MSL 3	SAT & Open/Short test Passed
TC (-55~125°C)	500 cycles: Open/Short Passed 1000 cycles: Open/Short Passed
HTS (150°C) w/o pre-con	500 hrs: Open/Short Passed 1000 hrs: Open/Short Passed
uHAST (130°C/85%RH)	96 hrs: Open/Short Passed

Figure 5: Reliability results for a GoM package.

maintaining manufacturing feasibility and maturity.

The reliability testing phase was conducted to evaluate the performance and durability of the GoS OBGA package under stringent automotive stress conditions, ensuring compliance with AEC-Q100 Grade 2 standards. The assessment included moisture sensitivity level 3 (MSL3), temperature cycling (TC), high-temperature storage (HTS) testing, and unbiased highly-accelerated stress testing (uHAST) to validate the package's environmental resilience and long-term reliability (see **Figure 4**).

The TC test subjected the package to extreme thermal fluctuations from -55°C to 125°C for 1000 cycles—testing its ability to withstand repeated thermal expansion and contraction. The HTS test—conducted at 150°C for 1000 hours—confirmed the package's long-term thermal stability. Additionally, uHAST was performed at 130°C and 85% relative humidity (RH) for 168 hours, assessing the package's resistance to moisture-induced degradation.

All samples successfully passed open/short circuit and scanning acoustic tomography (SAT) tests, with no failures or degradation observed. These results confirm the GoS OBGA package's suitability for automotive applications, demonstrating strong mechanical and optical reliability, as well as excellent resistance to environmental stress factors.

Glass-on-mold development

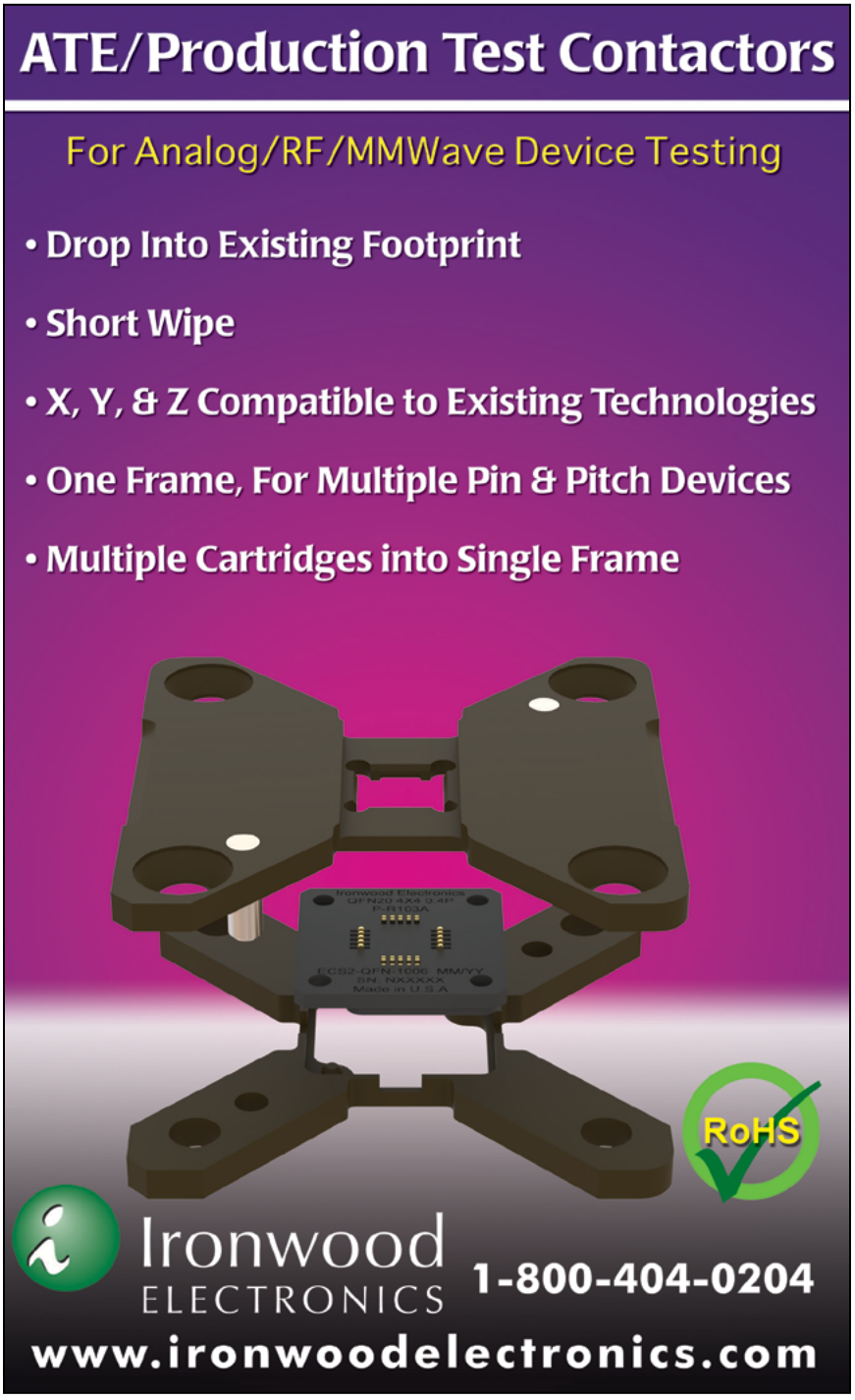
The experimental phase of development involved simulating various package configurations and materials to optimize the GoM OBGA package. The feasibility study focused on several key parameters, including glass attach process parameters, bond line thickness (BLT) and glass tilt management. These parameters were evaluated through a series of design of experiments (DOE) and simulations.

Several equations were used to guide the design process, including Boyle's Law, Charles's Law and Gay-Lussac's Law. These laws helped to understand the relationships between pressure, temperature and volume, which are critical for designing the cavity volume and controlling the process temperature.

The first step in the experiment was to identify preliminary design rules and package configurations that refer to MEMS's product initially. This involved creating study legs to run simulations and narrow down the package development scopes. The simulations considered factors such as bond line thickness of the glass adhesive and the contact width of the glass and glass adhesive material selection.

The simulation analyzed stress and design factors, such as the bill of materials and levels. The preliminary package configuration was reviewed based on the end application requirements, and a simulation DOE was conducted to evaluate different package sizes, glass adhesive materials, and bond line thickness levels.

The simulation results revealed two major weaknesses: the interface between the glass and glass adhesive layer, and the stress between the mold and solder resistance on the substrate. These weaknesses were addressed by optimizing the bond line thickness of the glass adhesive and its contact width, resulting in reduced glass stress and improved



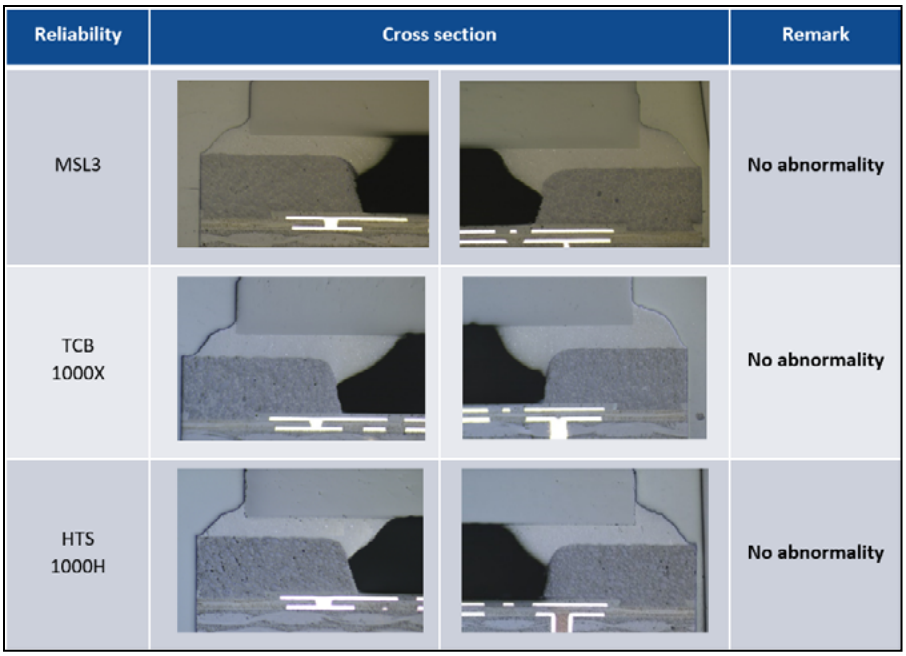


Figure 6: Package cross section after reliability testing of the GoM package.

reliability.

The feasibility study involved a series of tests to determine the optimal package configuration and process parameters. The DOE for the feasibility study was structured based on simulation data and included four legs with different glass contact widths and bond line thicknesses.

The key process optimizations identified during the feasibility study included die attach, wire bonding, solder ball attach, and package singulation. The wire bonding process, for example, was optimized to ensure reliable connections between the die and the substrate.

The glass attach process was a critical focus of the feasibility study. Three major metrics were evaluated: water infiltration, bond line thickness, and glass tilt. These metrics were essential for ensuring a completed sealed cavity to protect the sensor component and fulfill the flatness requirements for optical performance.

After process optimization, the GoM OBGA package underwent a series of rigorous reliability tests to ensure its performance for automotive applications, including TC, HTS testing, and uHAST (see **Figure 5**). The package was subjected to -55°C to 125°C for 1000 cycles, 150°C for 1000 hours, and 130°C/85% RH for 96 hours—all of which tested its resistance to thermal, humidity, and moisture stress. All samples passed the open/short and SAT tests, demonstrating no degradation or failure. These results confirm that the GoM OBGA package exhibits exceptional reliability, making it suitable for automotive applications that demand long-term stability, high performance, and environmental resistance.

To ensure package robustness, an integrity check was conducted to verify the interface between the glass-to-glass adhesive, mold top surfaces, and mold compound to substrate. The results confirmed no abnormalities after undergoing MSL3 preconditioning, 1000 cycles of TC, and 1000 hours of HTS, as shown in **Figure 6**.

Future development

The new GoM OBGA package provides a reliable, high-performance solution for automotive optical sensors. However, further enhancements can optimize its performance and miniaturization for next-generation applications. One key development focus is reducing package size by applying glass adhesive material over the wire and utilizing film-assisted molding technology. This approach can achieve greater compactness while maintaining performance and reliability.

Another avenue involves multi-chip or sensor integration, requiring collaboration with customers to design system in package (SiP) solutions that incorporate radar, LiDAR, or artificial intelligence (AI)-enabled processors to make possible intelligent sensor capabilities for autonomous vehicles.

Summary

GoS and GoM OBGA packages offer reliable, high-performance solutions for automotive optical sensors, addressing key challenges in thermal stability, optical performance, and manufacturability. The new OBGA package platform enhances miniaturization and manufacturing efficiency while maintaining flexibility for sensor fusion integration. Having a broad packaging portfolio that supports high-speed computing chips, power management devices, memory, network components, and MCU controllers, enables further evolution into SiP solutions, as well as sensor fusion integration. This packaging addresses the current and future demands of ADAS and autonomous vehicle technologies.

Biographies

Weilung Lu is a Sr. Director, MEMS and Sensor BU at Amkor Technology, Inc., Tempe, AZ. He joined Amkor in 2015 and is currently responsible for Optical Sensor products business and package development. Prior to joining Amkor, he worked for Siliconware Precision Industries Co., Ltd. (SPIL) as a technical program manager supporting key US customers and in R&D developing wirebond and flip-chip products. Weilung is a Doctor of Engineering Management from the George Washington U. Email: Weilung.Lu@amkor.com

Adrian Arcedera is Sr. VP, Memory, MEMS and Sensor BU, at Amkor Technology, Inc., Tempe, AZ. He joined Amkor in 1997 and has authored multiple technical papers and has been granted multiple US Patents. He holds a degree in Chemical Engineering from the U. of the Philippines.

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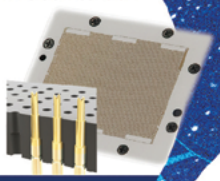

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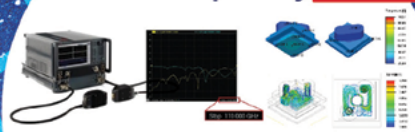
110GHz Actual Measurement Capability

Report in 3 Days!



Actual Measurement

2-Port: 110GHz

4-Port: 43GHz

Logic & SLT Socket

10 Sockets in 7 Days!

AI

Specification

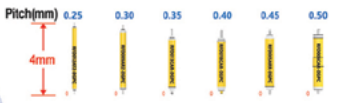
Frequency : 80GHz(BGA), 100GHz(QFN, LGA)

Pitch : 0.25mm~

Crosstalk : -60dB

Impedance : 50Ω±10%

1K Pins in 7 Days!



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kimmj@leeno.co.kr / +82 10 5314 6560

Direct laser reflow techniques for stable and reliable solder bump interfaces on semiconductor substrates

By Matthias Fettke, Anne Fisch, Thorsten Teutsch [PacTech – Packaging Technologies GmbH]

The purpose of this study is to introduce and qualify a contactless laser-assisted reflow (LAR) process for creating stable and reliable solder bump interfaces (C4) on semiconductor substrates offering a potential solution to minimize the CO_2 footprint of conventional oven-reflow processes. This work is a continuation of the studies by Fettke, et al. [1], and focuses on evaluating the lifespan of the generated solder joints.

Silicon (Si) chips and flexible FR4 substrates were used as test vehicles to evaluate the effects of the LAR process on a solder ball interface consisting of solder preforms made of SAC305 and Sn42Bi58. The 100µm and 400µm solder spheres were placed on the pads using a selective ball dropping process. For performance comparison, reference samples were prepared and conventionally reflowed in an oven. After the reflow processes, samples underwent various analyses to evaluate and compare the soldering quality. A 500-hour thermal cycling test was performed on the samples. Shear tests, X-ray, cross-sectional polishing, scanning electron microscopy (SEM) and optical microscopy were employed to examine the formation of the intermetallic compounds (IMCs) and the metallurgical properties of the solder bumps. Finally, industrialization proposals, possible application, and future prospects will be discussed.

Introduction

Conventionally, reflow ovens are used in mass production for forming solder bump interfaces on semiconductor substrates that rely on thermal conduction or convection requiring high volumes of inert gases like nitrogen to prevent oxidation. Preheating and gas flushing are essential to create an oxygen-reduced environment (<50ppm) for high-quality soldering. However, these methods consume significant "electrical" energy (8-12kW/h) and gas contributing to high CO_2 emissions. Therefore, alternative reflow processes are needed to reduce energy and gas consumption, as well as emissions.

With increasing efficiency and output power exceeding 25kW, laser systems are becoming a promising solution for improving the environmental sustainability of soldering processes. These systems generate the required thermal energy optically via short laser pulses typically in the near-infrared range; they offer reduced energy and gas consumption, as well as the ability to create dynamic reflow profiles and a smaller machine footprint. This has led to growing interest in laser-based reflow for forming solder bump interfaces in flip-chip applications. However, concerns remain about the stability and reliability of solder connections, including risks of peeling, burning, thermal stress, and weak IMCs. Further studies and proof of concept are needed to address these issues [1,2].

Process description

The sections below discuss the LAR process and provide an introduction to the test equipment used for the study.

Laser-assisted reflow. The selective LAR process utilizes a near-infrared (NIR) laser operating in the range of 980nm to 1070nm where semiconductor materials such as silicon and gallium arsenide exhibit low absorption. To ensure uniform reflow, the laser beam is optically modulated to create a consistent top-hat power distribution and its divergence is minimized to avoid localized heating inconsistencies. The beam profile is further adjusted through optical or mechanical means, thereby defining the final aperture. An infrared sensing system monitors and controls the substrate temperature, which requires calibration based on the material used.

The substrate with solder material like preforms, paste or plated layers, is placed on a stage and the laser heats the surface while the IR system regulates the temperature. Process gas is introduced to prevent oxidation during reflow, which typically lasts from 50ms to 10s, with the temperature set 20-30% above the alloy's melting point. The laser moves to different locations until all regions are processed. The process principle for reflowing a solder bump interface on a substrate level is illustrated in **Figure 1**.

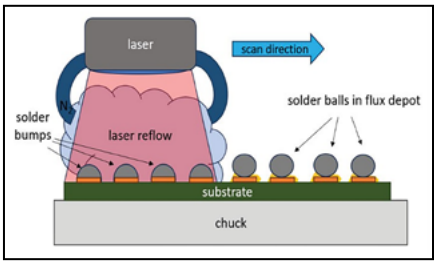

Figure 1: Principle behind the laser-assisted reflow (LAR) process.

The key benefits of LAR lie in its localized, selective, semi-transparent and highly dynamic reflow capabilities that minimize thermal impact on the substrates, thereby reducing mechanical stress in the forms of local and global warpage. Furthermore, it is expected to enhance the IMC's properties regarding size and grain structure resulting in longer-lasting interconnects as highlighted by Fettke, et al. [3] and Nishikawa, et al. [4].

Introduction to the test equipment. The solder bump laser reflow process was tested using a Laplace-Compact laser bonder from Pac Tech, equipped with a 1030nm Yb: YAG fiber laser delivering 1kW of optical output power. The system features an optical modulation setup enabling continuous adjustment of the laser spot size from 500µm x 500µm to 4cm x 4cm. For the comparison with a conventional reflow process, an AVT SRO-716 oven was used. **Figure 2** provides an overview of the test equipment used in the experiment.

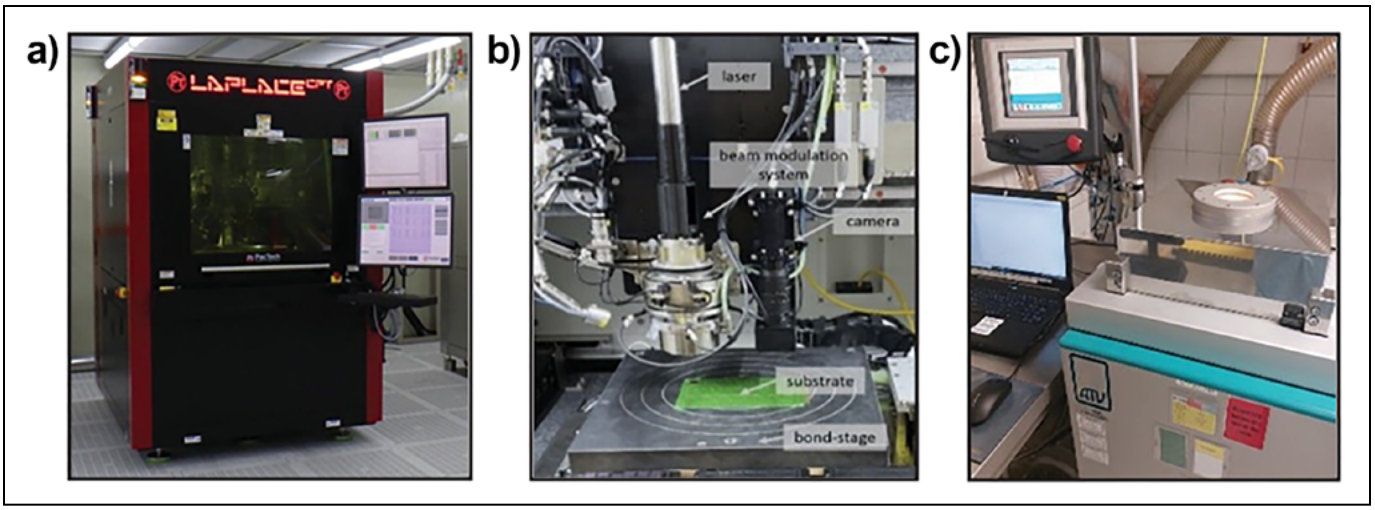

Figure 2: Test equipment used for the reflow study: a) (left) Pac Tech laser reflow system; b) (center) Detail of the laser reflow test setup; and c) (right) AVT SRO-716 reflow oven.

Regarding the laser reflow system, the spatial power distribution was evaluated using an Ophir SP11059 analyzer. The modulated beam profile used in the tests showed 90% beam homogeneity in accordance with DIN-ISO 13694 3.2.11. **Figure 3a** shows the modulated laser beam (pilot laser) covering a test area on the printed circuit board (PCB) test vehicle, and **Figure 3b** shows the measured spatial power distribution at a wavelength of 1030nm.

The output energy was measured using an Ophir L40(150)A laser power sensor. A high-speed Optris CTvideo pyrometer was used to characterize the LAR process, allowing both temporal and thermal analyses. The chosen 3MH-CF pyroelectric sensor has a measurement range of 100°C to 600°C, a spectral range of 2.3µm, a temperature resolution of 0.1K, and a 1ms time resolution. The emissivity coefficient (c) was set to 0.25 for Sn [1,5].

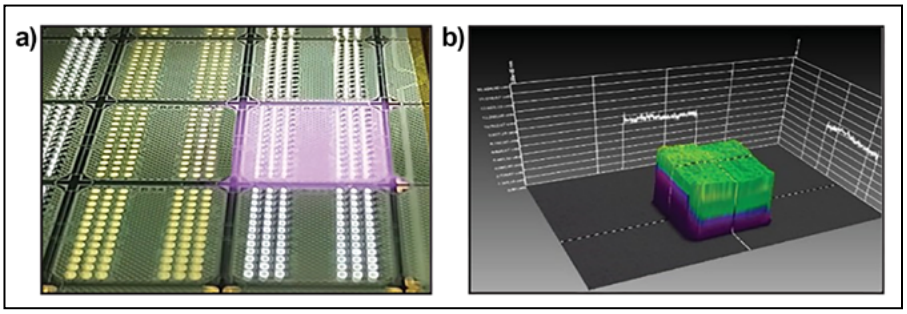

Figure 3: Laser tool beam characteristic: a) (left) Modulated laser beam on a substrate (pilot laser); and b) (right) 3D profile.

sample type	picture	pad count	sample size	pad dia	plating
Si chip		572	10 x 10 mm²	100 ± 2 µm	e-plated Al 20µm Ni 5 µm Au 40 nm
FR4 PCB		78	10 x 12 mm²	350 ± 15 µm	e-less Cu 15 µm Ni 10 µm Au 20 nm

Figure 4: Overview of test samples that were used.

Experimental

The following sections describe test sample preparation, optical inspection, cross-sectional analysis of the samples, mechanical analysis shear test results, and X-ray analysis of the test vehicles.

Test sample description and preparation. The test substrates used in this study consist of both organic and inorganic materials showing a symmetrical plated pad structure. Detailed information about the test vehicles is presented in **Figure 4**.

To prepare the test substrates in order to match a conventional solder ball transfer process, an 8µm sticky flux film (Kester TSF-8818HF) was applied using a manual squeegee (Zehntner ZUA 2000). SAC305 and Sn42Bi58 solder balls of 400µm were sequentially placed on the printed circuit board (PCB) test parts, and 100µm solder balls on the Si chip utilizing a sequential dropping process as illustrated in **Figure 5**.

To find a suitable starting point, the shortest laser energy process window was identified based on shear tests that showed a cohesive fracture mode. From this minimal setting, the laser pulse length

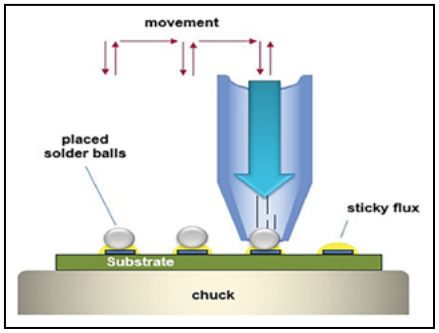

Figure 5: Principle of the ball dropping process.

substrate type	alloy	sphere dia. in µm	temp. limit in °C	min. laser energy in J/mm²	laser reflow in s				
Si-Chip	SAC_305	100	250	0.56	0.75	1	2	3	4
	Sn42Bi58	100	170	0.45	0.5	1	2	3	4
PCB	SAC_305	400	250	0.56	0.75	2	3	5	7
	Sn42Bi58	400	170	0.45	0.5	2	3	5	7

Figure 6: Test matrix for the LAR process study.

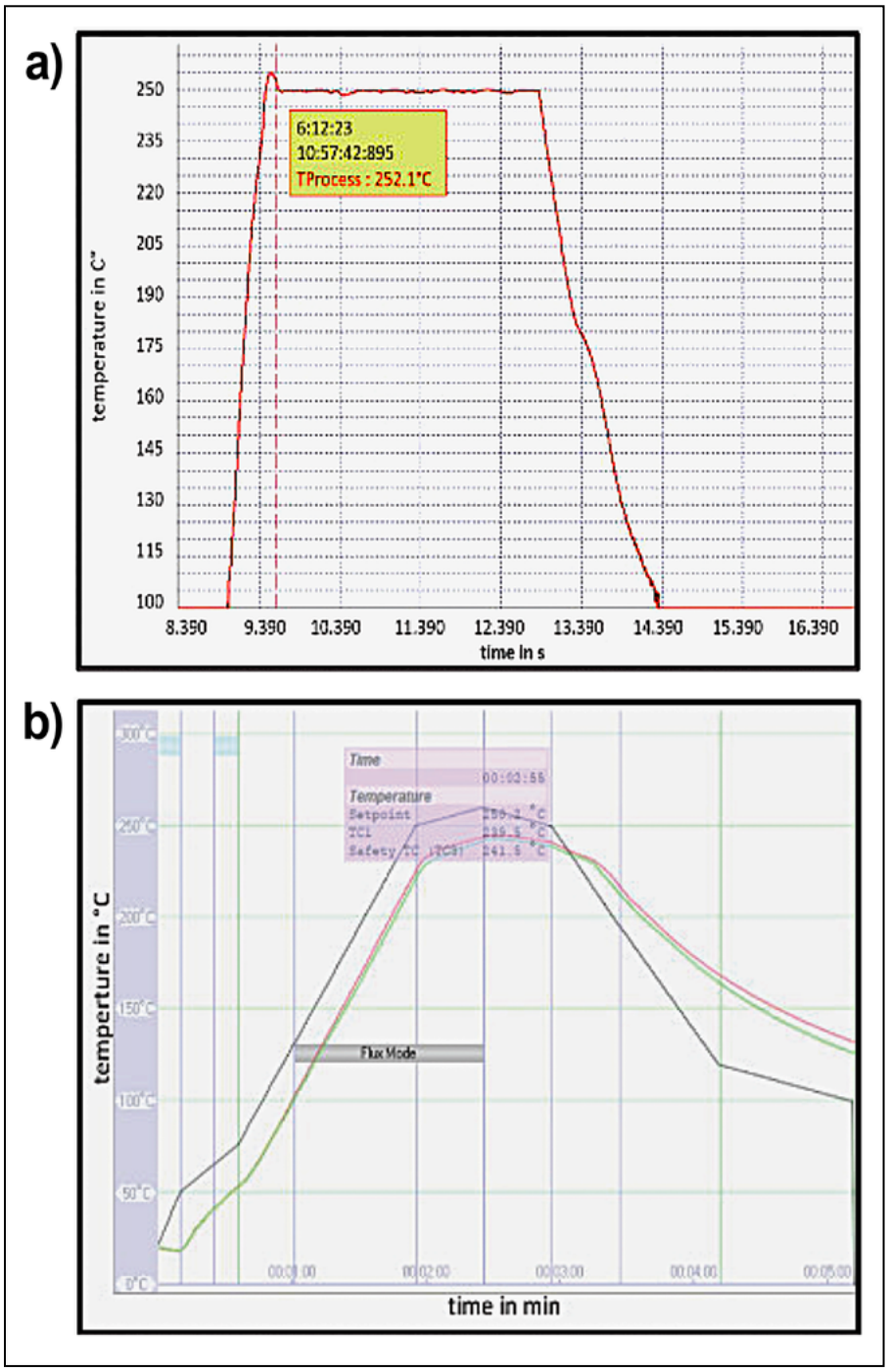

Figure 7: Examples of 400µm SAC305 reflow profiles on a PCB test sample before thermal cycling: a) (top) 1s laser-reflow; and b) (bottom) Oven reflow.

was gradually increased and the solder bump interface condition was assessed for five different laser reflow times. The test matrix and the minimum identified laser energy density for all laser energy configurations are shown in **Figure 6**.

During the laser reflow process, the laser spot was modulated to irradiate the ball-populated area on the test units (1mm x 1.2mm for the PCB and 1mm x 1mm for the Si chip) at a distance of 1cm with a power of 90W. A nitrogen shower set at 120mbar protected the soldering area from oxidation. Peak temperature limits were maintained at 250°C for SAC305, and 170°C for Sn42Bi58. An example of a 4s laser reflow profile measured with a pyroelectric sensor system on a 400µm SAC305 bump array on a PCB sample is shown in **Figure 7**. The temperature profile exhibits a three-stage characteristic with an extremely high heating rate of 500°C per second, followed by a constant temperature maintained throughout the holding time, and finally, the cooling of the substrate after the system is turned off.

For comparison with conventional reflow processing, reference samples were prepared identically, but underwent the reflow in an AVT SRO-716 oven. For SAC305 solder spheres, the peak temperature was set to 250°C, while for Sn42Bi58, it was set to 170°C. The total reflow time was 400s for SAC305 and 300s for Sn42Bi58. **Figure 7** shows the used oven reflow profile for the SAC305 alloy. Five samples were produced for each of the reflow test configurations that were subsequently qualified using metrological methods [1].

Optical inspection. After completing the reflow process steps and the initial measurement analysis, the test vehicles were subjected to a thermal stress test. Following the stress test, the samples were reanalyzed and the results were compared. The temperature cycling test was conducted in a 2-zone oven according to DIN EN 60062-2-14:2010-04 to assess and compare the degradation mechanisms of laser- and oven-reflowed solder bumps. The CTS TSS-70/130 thermal cycling system served as the measurement apparatus with temperatures ranging from -40°C to +125°C. The samples underwent 500 thermal cycles with a 30-minute hold time in each chamber under standard atmospheric conditions.

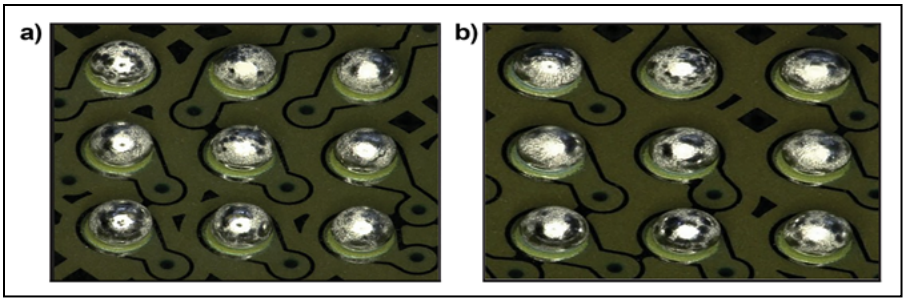

Figure 8: Examples of 400µm SAC305 reflow profiles on a PCB test sample before thermal cycling: a) (left) 1s laser-reflow; and b) (right) Oven reflow.

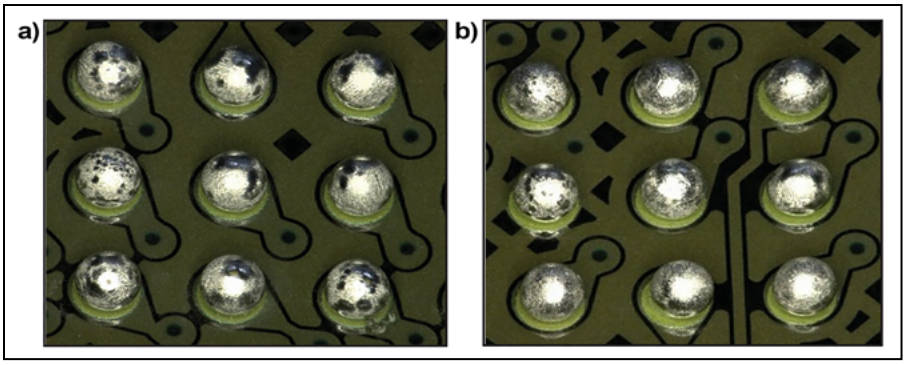

Figure 9: Examples of 400µm SAC305 reflow quality on a PCB test sample after thermal cycling: a) (left) 1s laser reflow; and b) (right) Oven reflow.

The solder bump reflow results were optically inspected and compared using a digital Keyence VHX 950F 3D microscope. Examples of the inspection results for 1s laser-reflowed and oven-reflowed SAC305 solder bumps on the PCB samples before and after thermal cycling are shown in **Figures 8** and **9**.

As can be seen, the solder bumps exhibited no structural defects and demonstrated complete pad coverage with uniform shape and surface quality alongside the characteristic tarnished appearance expected of such joints. No discernible optical differences in surface condition were observed between the laser-reflowed and oven-reflowed SAC305 and Sn42Bi58 solder bumps—nor were any differences observed on the PCB samples, nor on the Si chips. However, after the thermal cycling test, the oven-reflowed test samples exhibited a slight increase in optical tarnish indicating increased surface roughness, while the laser-reflowed samples remained cosmetically unchanged.

Additionally, all laser-reflowed solder bumps showed an identical optical appearance regardless of selected pulse length. The substrate surfaces exposed to laser irradiation between the contacts also remained unaffected by thermal damage, showing no signs of delamination, cracking or tarnishing effects either before or after the thermal cycling [1].

Cross-sectional analysis. A cross-sectional analysis was performed on the processed samples to evaluate size and shape of the IMCs and metallurgical structure of the formed solder bumps. The solder bumps were carefully examined for cracks, voids, delamination and other structural irregularities using an Olympus MX61 light microscope and a Zeiss Neon 1540 EsB SEM. The IMC dimensions were measured with the scanning electron microscope (SEM) system. For this purpose, the samples were embedded, ground and polished. From analysis charts in **Figures 10** and **11** it is evident that the IMC has significantly increased in size for both solder materials after the thermal cycling test.

After the 500 cycles, the SAC305 IMC thickness increased from 952nm to 5.8µm on the oven-reflowed PCB samples, and increased from 1.78µm to 6.5µm on the Si chips. The Sn42Bi58

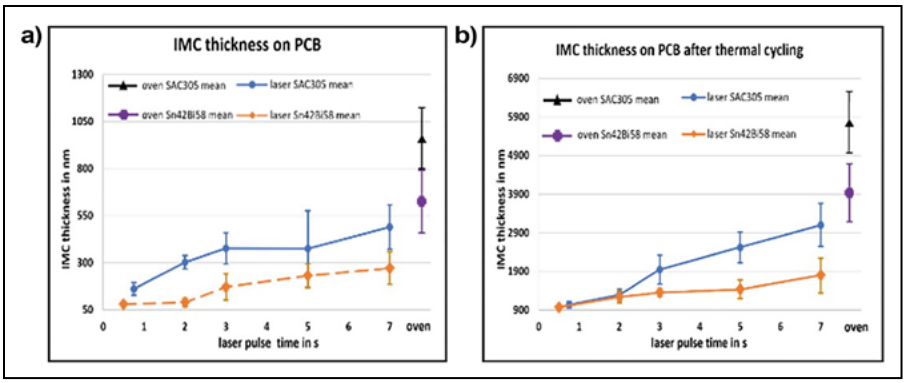

Figure 10: IMC thickness measurement at the solder/pad interface on a PCB: a) (left) Before thermal cycling; and b) (right) After thermal cycling.

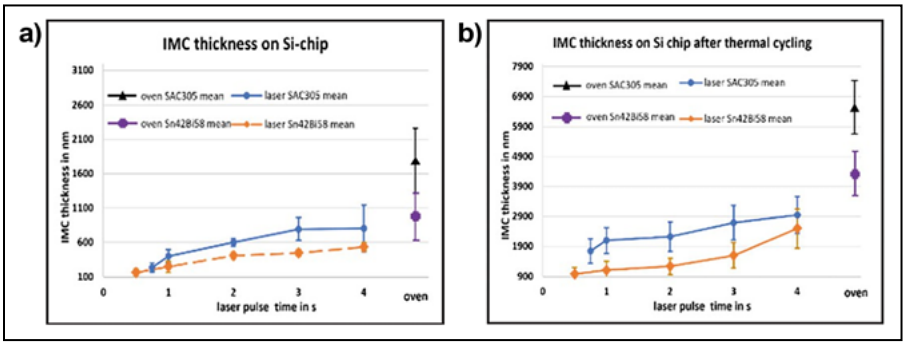

Figure 11: IMC thickness measurement at the solder/pad interface on a Si chip: a) (left) Before thermal cycling; and b) (right) After thermal cycling.

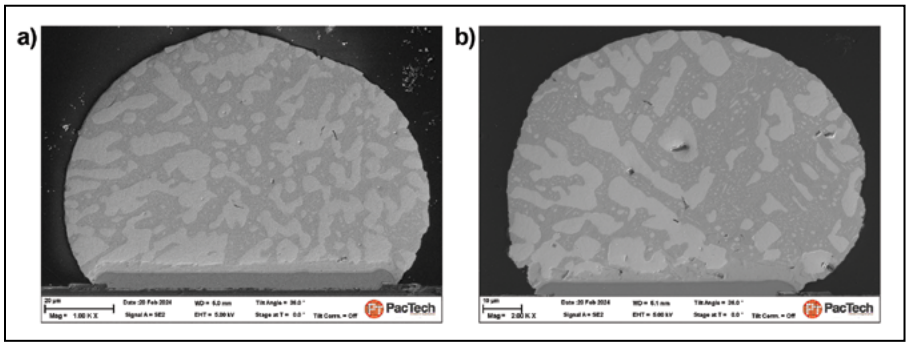

Figure 12: Cross-sectional SEM picture of a SnBi solder bump on a Si chip after thermal cycling: a) (left) 7s laser reflow; and b) (right) Oven reflow.

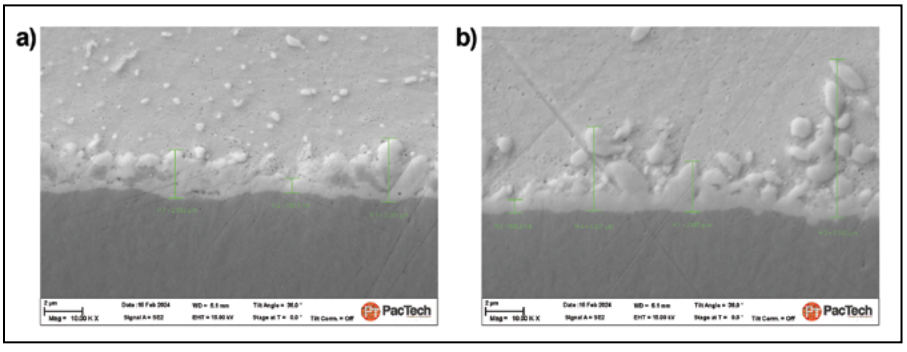

Figure 13: Cross-sectional SEM picture of an SAC305 solder bump on a PCB after thermal cycling: a) (left) 7s laser reflow; and b) (right) Oven reflow.

IMC thickness increased from 598nm to 4µm on the oven-reflowed PCB samples, and from 972nm to 4.2µm on the Si chips. The IMC layer for the laser-reflowed samples remained significantly smaller. However, when the 4s-laser pulse was used, an increase from 782nm to 2.9µm for the SAC305 solder bumps, and from 591nm to 2.4µm for Sn42Bi58 bumps on the Si chips, was achieved. The IMC thickness on the PCB samples increased from 458nm to 2.2µm for the SAC305, and from 284nm to 1.4µm for the Sn42Bi58 solder alloy.

Figures 10 and **11** also show the correlation between optically-induced thermal energy and growth characteristics. An almost linear correlation is present and coincides with the results described by Dusek, et al. [10]. The elevated standard deviation observed around each measurement point—which escalates with increasing energy—suggests an augmentation in the irregularity of IMC shape. The data showed that the Sn42Bi58 alloy formed shorter IMCs compared to the SAC305, which is consistent with findings in [10] and [13].

Consequently, it can be concluded that the laser-formed solder joints do not exhibit any detrimental characteristics regarding stability and reliability compared to the oven-reflowed solder contacts. Moreover, it can be assumed that the reduced IMC growth during the thermal stress test in the laser-formed contacts results in a longer lifespan of the solder joints.

Figure 12 shows an example of the different grain sizes after the thermal cycling test for the Sn42Bi58 contact on the Si chip. It is evident that the crystal structure in the solder volume is significantly finer in the laser-reflowed solder bulk compared to the oven-reflowed formed solder structure. This explains the more tarnished surface structure observed in **Figures 8** and **9** on the oven-reflowed solder bumps.

Figures 13 and **14** show examples of the structure and shape of the formed IMC. The two-layered IMC system consisting of Ni3Sn4 and the subsequently grown and more pronounced AuSnNiBi phase, as described by Kang, et al. [6], became clearly visible. No metallurgical defects were found in the bulk material in any of the samples before and after the thermal cycling test during the SEM inspection [1].

Mechanical analysis shear test. To evaluate the mechanical properties, shear tests were conducted using a Dage BT 4000 shear tester in accordance with the JEDEC standard [9]. The bumps were sheared at a speed of 0.2mm/s with a shear height of 9µm. Fractures in the joints were examined and classified via optical inspection using an Olympus MX61 light microscope. **Figures 15-18** present examples of the resulting fracture modes at the 100µm solder bump interface of the Si chips for both the SAC305 and Sn42Bi58 alloys before and after thermal cycling. The observed fracture modes in all measured samples consistently exhibited cohesive shear failure. Additionally, the fracture morphology across the entire laser energy range for each specific solder alloy/substrate configuration displayed a consistent pattern.

Compared with the results presented in **Figures 15** and **17**, a difference in appearance is obvious after the thermal cycling. For the SAC305 solder, the morphology shows an initial shear portion of around 35-40% before transitioning to a peeled fracture. This is attributed to the higher grain size after thermal cycling, which reduced the ductile portion of the SAC305 material. The solder became harder resulting in increased resistance to compression and leading to this type of fracture pattern and decreased shear force. Similar characteristics were observed for the Sn42Bi58 solder. The small initial shear fracture disappeared leaving a 100% brittle fracture.

On the PCB samples, all 78 solder bumps were sheared. Similarly, on the Si chips, 78 out of 572 locations evenly distributed across the entire bump array were sheared. For the PCB samples with 400µm solder bumps, the minimum shear force was calculated at 359.52gf for the SAC305 alloy, and 495.77gf for the Sn42Bi58 alloy. For the Si chips with 100µm solder bumps, the minimum shear force was calculated to be 30.76gf for the SAC305 alloy, and 42.43gf for the Sn42Bi58 alloy. The shear test results presented as mean values for different laser reflow pulse widths and for the oven-reflowed SAC305 and Sn42Bi58 bump interfaces on the PCB samples before and after thermal cycling, are shown in **Figure 19**. **Figure 20** displays the corresponding results for the Si chips [7,8].

The thermal cycling stress test led to a reduction in shear strength across all

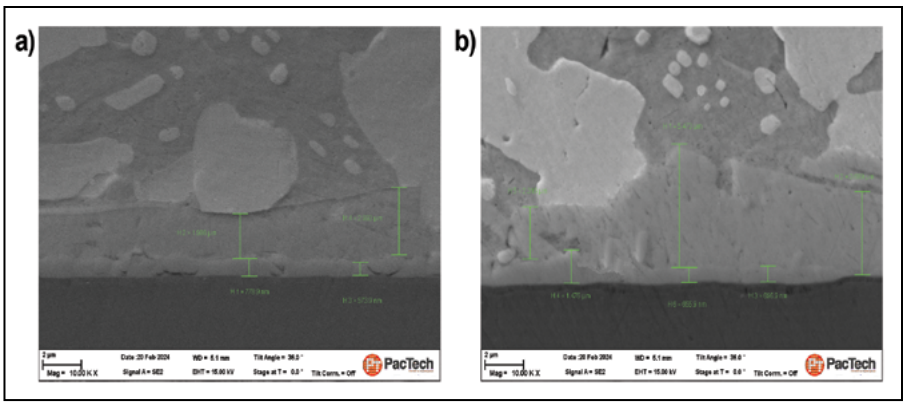

Figure 14: Cross-sectional SEM picture of a SnBi solder bump on a Si chip after thermal cycling: a) (left) 7s laser reflow; and b) Oven reflow.

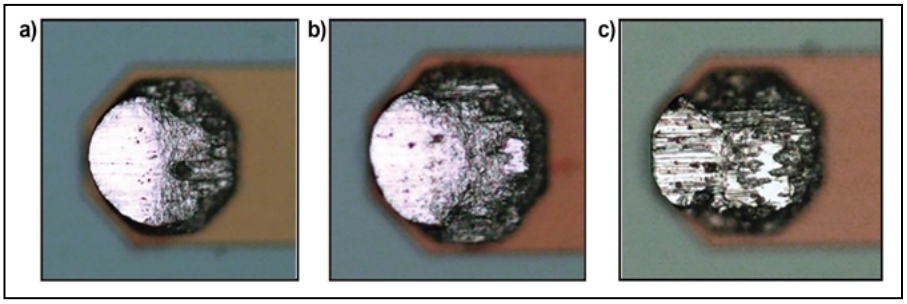

Figure 15: SAC305 shear test fracture modes on a Si chip before thermal cycling: a) (left) 750ms laser reflow; b) (center) 4s laser reflow; and c) (right) Oven reflow.

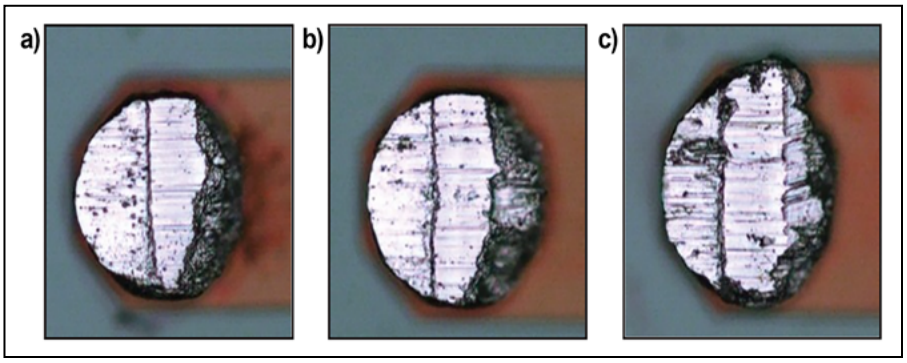

Figure 16: SAC305 shear test fracture modes on a Si chip after thermal cycling: a) (left) 750ms laser reflow; b) (center) 4s laser reflow; and c) (right) Oven reflow.

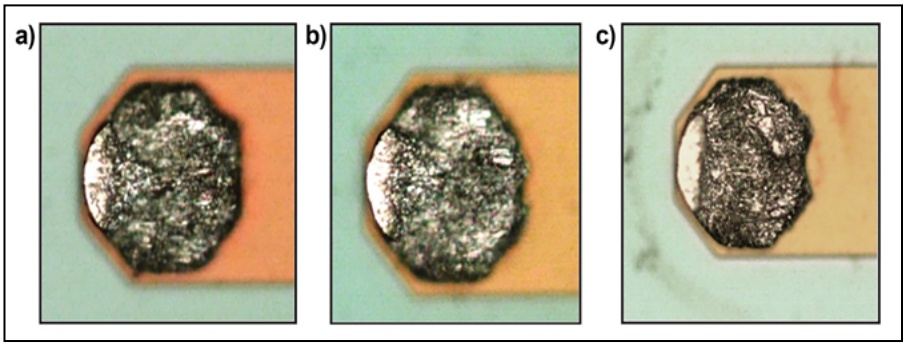

Figure 17: Sn42Bi58 shear test fracture modes on a Si chip before thermal cycling: a) (left) 750ms laser reflow; b) (center) 4s laser reflow; and c) (right) Oven reflow.

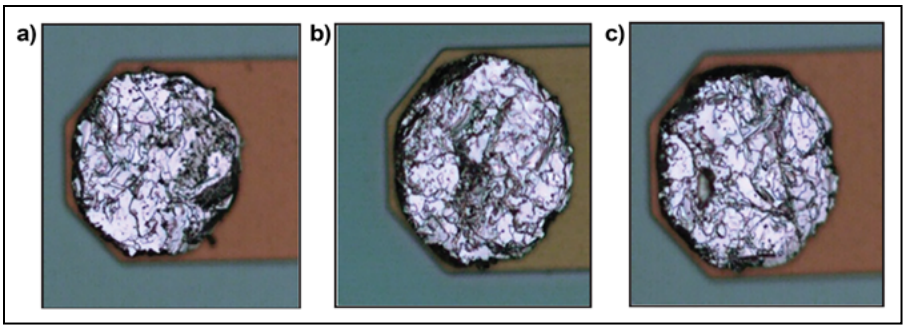

Figure 18: Sn42Bi58 shear test fracture modes on a Si chip after thermal cycling: a) (left) 750ms laser reflow; b) (center) 4s laser reflow; and c) (right) Oven reflow.

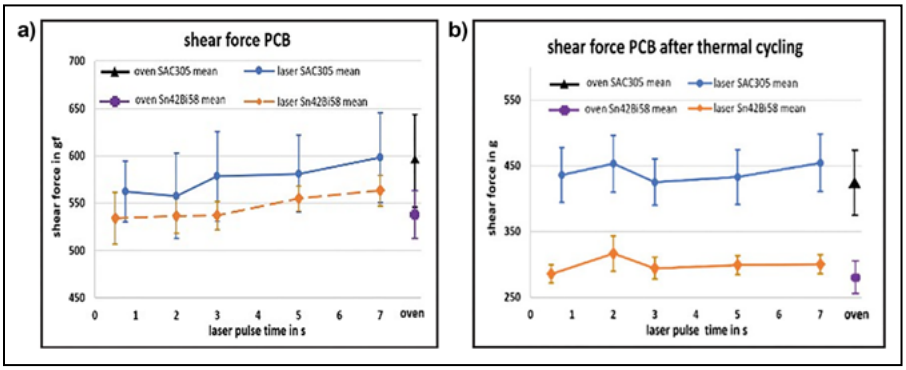

Figure 19: Shear test results for the solder interface on a PCB sample: a) (left) Before thermal cycling; b) (right) After thermal cycling.

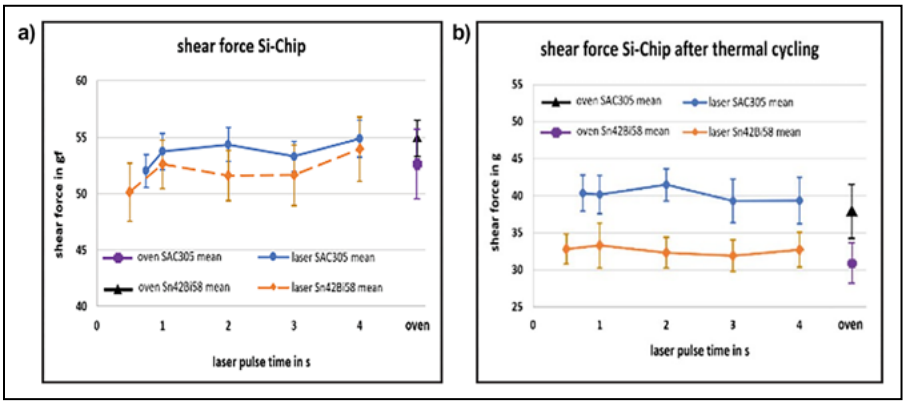

Figure 20: Shear test results for the solder interface on a Si-Chip sample: a) (left) Before thermal cycling; b) (right) After thermal cycling.

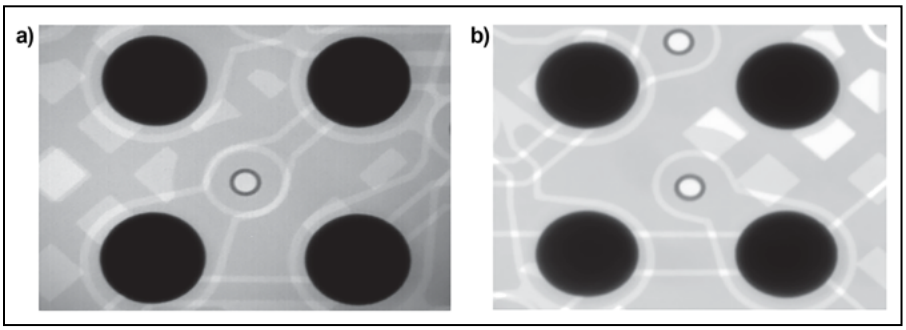

Figure 21: X-ray measurement results of an oven-reflowed 400µm SAC305 solder bump interface on a PCB: a) (left) Before thermal cycling; and b) (right) After thermal cycling.

sample configurations. Samples soldered with Sn42Bi58 fell below the minimum shear strength threshold. Furthermore, after thermal cycling, all convection oven-soldered samples exhibited lower shear strength compared to their laser-soldered counterparts. No notable differences in shear strength were observed among the samples subjected to different laser parameters. The substantial reduction in shear strength in the Sn42Bi58 samples is attributed to the diffusion of Ni from the pad metallization into the solder joint, which results in increased embrittlement and the loss of the primary ductile component. Replacing Ni with Cu in the pad metallization would mitigate this issue [11-13].

Generally, all mean values lie within the error bar/standard deviation of the corresponding oven-reflowed mean shear force, which provides an initial indication of a non-negative impact on the mechanical stability and reliability of the laser-reflowed solder bump array before the thermal cycling. The results of the analyses after the thermal cycling indicate that the laser-soldered samples show significantly improved metallurgical properties compared to the oven-reflow solution. A more stable and reliable contact interface for semiconductor components can be expected [1].

X-ray analysis. The solder bumps were analyzed using an X-ray system to detect voids or any irregularities within the solder material, at the interface, and in the adjacent substrate materials. Comparative measurement results between laser reflow and oven reflow before and after the thermal cycling are illustrated in **Figures 21** and **22** for the SAC305 bump array on a PCB test vehicle. The results show no evidence of voids or structural defects in the solder bump bulk. X-ray inspections revealed no significant quality differences between the laser-reflowed solder bumps and the oven-reflowed reference samples before and after the thermal stress test [1].

Summary

The metrological analysis of the thermally-cycled solder contacts showed that contactless LAR produces stable and reliable bump interconnects that fully meet the lifetime expectations of conventionally oven-reflowed produced solder bump interfaces, within the examined qualification range.

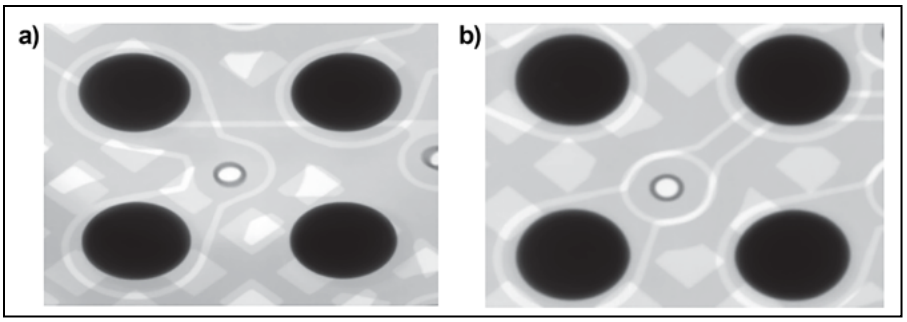

Figure 22: X-ray measurement results of a 2s laser-reflowed 400µm SAC305 solder bump interface on a PCB: a) (left) Before thermal cycling; and b) (right) After thermal cycling.

Moreover, the obtained results showed higher shear strength and an improved metallurgical structure suggesting a longer lifespan for the laser-formed solder contacts after the thermal cycling test. The increased thickness initiated by the thermal cycling for the Sn42Bi58 IMC layer on the Si chips can be calculated to be 6.68 for the oven-reflowed, and 4.06 for the laser-reflowed test samples.

With significantly shorter reflow times, which in this study ranged from 500ms to 7s, there is a high potential for cost reduction due to minimized energy and N_2 consumption, and consequently, a reduction in CO_2 emissions becomes apparent. Additionally, the machine footprint—an important cost factor for cleanroom infrastructure—is significantly smaller. The conventional large zone oven can easily be replaced by a standalone laser-reflow system, achieving similar cycle times. If one considers a 100 x 100mm^2 laser spot size and a 2s pulse duration to reflow a 300 x 300mm^2 panel, that would mean a total reflow time of 18s would be required. In comparison, with a typical belt speed of 1.33cm/s in a 10-zone oven, the cycle time would be 23s [14].

Furthermore, efforts are being made to scale up the laser spot size to 150mm x 150mm and the process will be qualified for reflowing surface-mount technology (SMT) components and assembling chiplets. The assembly of chiplets with solder contacts smaller than 16µm in particular requires processes that induce minimal thermal stress. On one hand, the growth of IMCs must be minimized to ensure a sufficient amount of ductile material remains in the joint, while on the other hand, both local and global warpage must be prevented.

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Biographies

Matthias Fettke is VP, Advanced Packaging Equipment at PacTech – Packaging Technologies GmbH, Nauen, Germany. He is an expert on laser-assisted bonding technologies for semiconductor packages and electrostatic chucks used in the field of extreme ultraviolet (EUV) lithography. He holds a Master's degree in Laser- & Optotechnologies from the U. of Applied Science Ernst Abbe; email fettke@pactech.de

Anne Fisch is a Microtechnologist at Pac Tech GmbH, Nauen, Germany. She works in process development for laser-assisted joining technologies and is an expert in metallurgical sample preparation and defect analysis.

Dual-damascene process for a 500nm RDL using a high-resolution photosensitive polymer

By Carine Gerets, Eric Beyne, Nelson Pinho, Wen Hung Tseng, Tinneke Paulus, Nouha Labyedh, Gerald Beyer, Andy Miller [imec]

This paper investigates the dual-polymer damascene process for the redistribution layer (RDL—focusing on the fabrication of lines and vias with dimensions as small as 500nm. This corresponds to an RDL line pitch of 1000nm, and a via-to-via pitch of 2000nm. The optimization of RDL lithographic process steps, achieved through the integration of a novel polymer, is presented in detail. These optimized processes enable the formation of functional M1-VIA1-M2 chains, with up to 450 blocks successfully fabricated at dimensions of 500nm, 700nm, and 1000nm. The scaling of both RDL lines and vias is approaching the standard 400nm dimensions commonly employed in silicon interposers.

Introduction

Traditional semiconductor chips are based on monolithic designs in which all functionalities are integrated onto a single chip. However, this design approach has limitations, including high production costs, limited die size (lithographic reticle limit) and diminishing returns in efficiency and scalability. A novel solution to these challenges is a technology that partitions complex chips into smaller segments known as chiplets. It becomes possible to aggregate chiplets with individually-optimized process nodes, technology design and materials. Smaller individual dies and higher volumes due to reutilization lead to much higher yields and reduced costs. The effectiveness of chiplet strategy is contingent upon the quality of the chiplet interconnections. To achieve optimal performance, various strategies for interconnect aggregation can be employed, such as silicon interposers, silicon bridges, and RDLs, each of which addresses different performance and cost considerations [1-7].

The semiconductor industry moves more and more to faster devices—and the devices demand higher bandwidth to achieve a higher data transfer rate. Bandwidth is a function of the interconnect density and the possible transfer speed per line. The industry has the need to increase bandwidth as well as have lower power consumption. In this paper, we present our ongoing work on the RDL interconnect strategy, specifically focusing on the development of a higher 3D interconnect density of a polymer RDL. This is achieved through two primary interdependent strategies. The first involves increasing lateral line density with our current demonstration of a line/space of 500nm [1,7]. The second strategy focuses on enhancing the areal (vertical) density by improving inter-layer connection densities. In this study, we introduce via pitch solutions as small as 2000nm, with individual via dimensions down to 500nm.

To demonstrate our results, we utilize two metal layers interconnected by a via layer (M1-VIA1-M2). We perform electrical characterization on an assortment of test structures within our test vehicle, with a gradient of feature dimensions down to 500nm.

Process description

The complete M1-VIA1-M2 stack is constructed first with a single polymer damascene M1 layer followed by polymer dual-damascene VIA1-M2 layers. All layers utilize a high-resolution phenol-based negative-tone i-line photosensitive polymer manufactured by JSR Corporation. It belongs to the commercial family ELPAC™ WPR series. The lithographic process is performed on an ASML ASM200 i-line (365nm) stepper with a numerical aperture (NA) of 0.48. The standard development process is performed with diluted TMAH followed by a full cure in a nitrogen environment

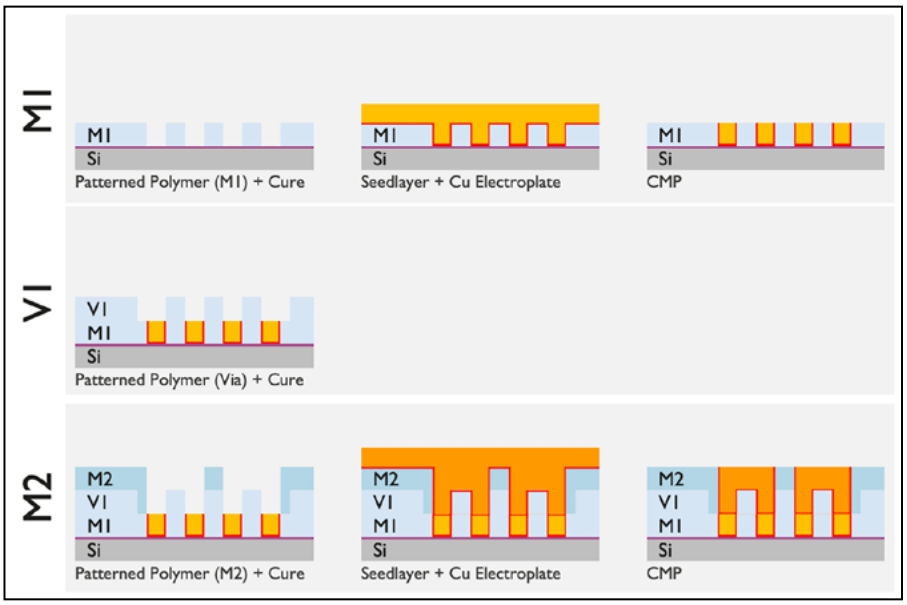

Figure 1: Schematic overview of the damascene process: Single polymer damascene M1 layer followed by polymer dual-damascene VIA1-M2 layers.

at 200°C for 1 hour with additional temperature ramp-up/ramp-down to room temperature (RT).

As exemplified in **Figure 1**, the first single-damascene M1 layer has a patterned M1 polymer layer. This is followed by a very short descum and sputtered Ti/Cu=30/150nm seed layer. The open M1 areas are then over-plated using a bottom-filled electrolyte. The final metal lines are revealed with a two-stage chemical mechanical polish (CMP) process. The first stage uses a highly-selective copper polish to remove excess copper, and the second stage involves barrier/polymer removal with non-selective slurry.

For the subsequent VIA1 and M2 layers, the process follows a polymer dual-damascene approach. Each polymer layer is sequentially patterned and cured. The M2 layer overlaps with the open areas of the VIA1 layer. This is illustrated in **Figure 1**, where the M2 layer is depicted in a slightly darker shade of blue to highlight the truncation of the vias. Truncation may occur either due to overlay misalignment, or by intentional design. An intentional truncation strategy assists lithographic process capability as it allows for more relaxed CDs for the most critical via structures and extends overlay tolerances between layers [8]. The metallization process for VIA1 and M2 mirrors that of M1, involving seed layer deposition followed by the electroplating of VIA1 and M2. The entire stack (M1, VIA1, and M2) is fully planarized using a compound CMP process.

In this study, two distinct polymer film thicknesses were applied: FT=1.3µm and FT=2.0µm. Given that polymer performance is characterized by a thickness-to-critical dimension (CD) aspect ratio (AR) of approximately 2.5 to 3, each thickness targets a different CD. The FT=1.3µm thickness is designed for a target CD of 500nm, while FT=2.0µm targets a CD of 700nm.

Development of the lithographic process steps

The following sections discuss process steps needed to generate the M1, V1A1, and M2 layers.

M1 layer. The lithographic process setup of the high-resolution polymer

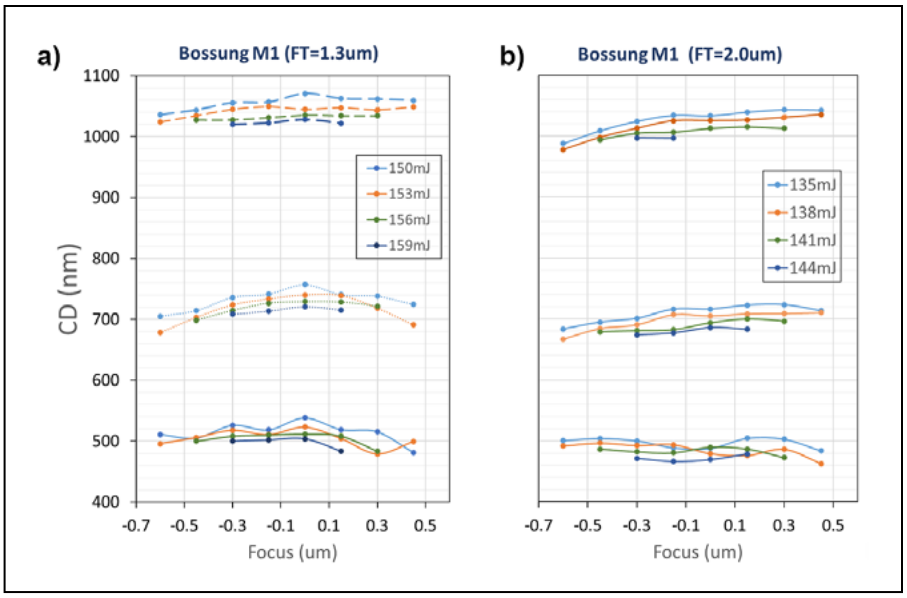

Figure 2: M1 Bossung curve for: a) (left) FT=1.3; and b) (right) 2.0µm.

for all layers is the most critical step in the entire process sequence. Focus exposure matrix (FEM) analyses were performed for each layer. **Figure 2** shows the Bossung curves for the M1 layer after the development for four main candidate exposures for each thickness. Three nominal line structures where reviewed (500nm, 700nm, and 1000nm). Bossung curves plot CD as a function of focus for each exposure set. Process windows can be qualitatively assessed. Fixed exposure conditions and exposure settings of 159mJ/cm^3 (FT=1.3µm) and 141mJ/cm^3 (FT=2.0µm) were selected.

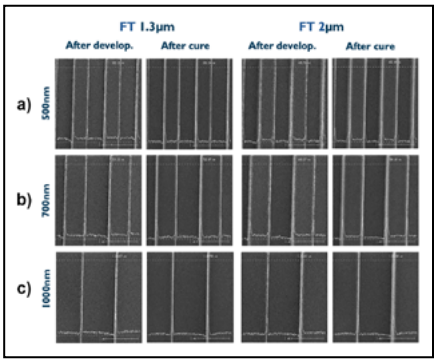

Figure 3: M1 Top SEM images before/after cure for: a) (top) 500nm; b) (middle) 700nm; and c) (bottom) 1000nm line structures for both FT=1.3µm/and 2.0µm.

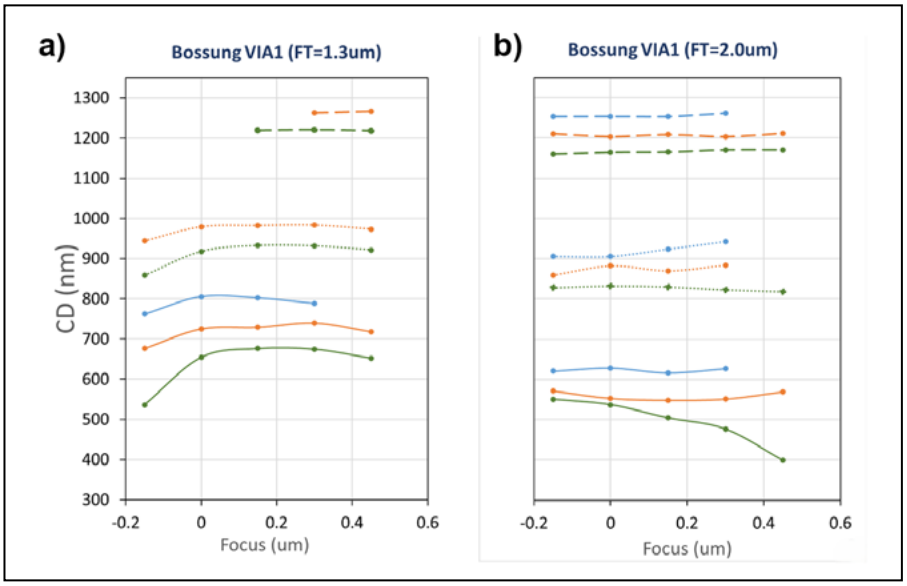

Figure 4: VIA1 Bossung curve for: a) (left) FT=1.3; and b) (right) 2µm after development.

Top scanning electron microscope (SEM) images of these conditions are presented in Figure 3—the low line roughness and vertical sidewall are visible in each panel of the figure. The curing of the polymer presents an FT shrink of ~8%.

VIA1 layer. For the VIA1 layer, FEMs were also performed for both FTs. In Figure 4 we have the Bossung curves for the main exposure settings. The process window for the via lithographic process is smaller than that for line patterning. This is also observed (Figure 5) in the rounding of the designed square vias. Due to the adaptation of a truncation strategy, the target CD for each via is not the nominal value in the design, but rather the via process was shifted to be ~40% larger. This shift would assist in process capability as well as overlay variance. The M2 layer will truncate the vias in the subsequent process block. Finer granularity for the VIA1 design of experiment (DOE) CD was not available in the mask set utilized. Fixed exposure conditions,

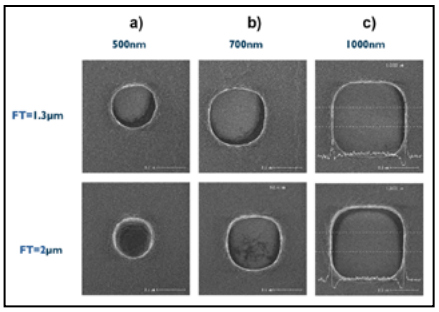

Figure 5: VIA1 top SEM images for: a) (left) 500nm; b) (middle) 700nm; and c) (right) 1000nm via structures for both FT=1.3µm/and 2.0µm.

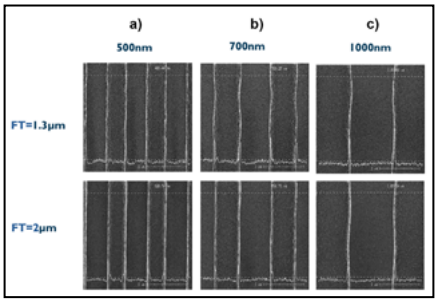

Figure 6: M2 top SEM images after cure for: a) (left) 500nm; b) (middle) 700nm; and c) (right) 1000nm line structures for both FT=1.3µm/and 2.0µm.

and exposure settings of 95mJ/cm^3 (FT=1.3µm) and 85mJ/cm^3 (FT=2.0µm), were selected.

M2 layer. Similar to the previous layers, an FEM was performed on the M2 layer. Here, some waviness was observed in the line structures in the FEM wafer. The criteria for fixed conditions here was not only the target CD, but also adequate truncation via openings with a reduced number of residues. Fixed exposure conditions, exposure settings of 124mJ/cm^3 (FT=1.3µm) and 101mJ/cm^3 (FT=2.0µm) were selected being on the high side of the Nominal±10% CD acceptance range.

The standalone M2 lines are presented in Figure 6. Also, in Figure 7, the top SEM images of the chain structures can be seen. The M2 layer truncation of the underlying slightly enlarged vias can also be seen.

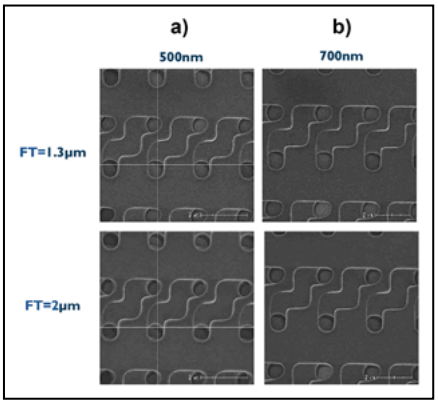

Figure 7: VIA1+M2 top SEM images after cure for: a) (left) 500nm; and b) (right) 700nm chain structures for both FT=1.3µm/and 2.0µm.

Characterizations of the RDL stack

The following sections discuss mask design, critical dimensions, overlay, and electrical results with respect to characterizing the RDL stack.

Mask design–VIA DOE. Following development work already published [7], enlarging via dimensions in a dual-damascene process facilitates the process critical via patterning. In addition to assisting the patterning process, overlay conditions are relaxed along the M2 openings. Overlay capabilities of the ASM200 are registered to be up to 200nm (±3α). Ideally, for a targeted 500nm CD, the process overlay capability should be an

order of magnitude smaller, permitting a low variance in the contact cross section. In the current mask set design, there exist type A vias in which the square vias have the same dimension as the underlying line CD. There is no landing pad or overlay budget. Type B vias have an elongation of one of the dimensions to double the length along the M1 metal contact. These conditions can be visualized in Figure 8 with the vias in dark red.

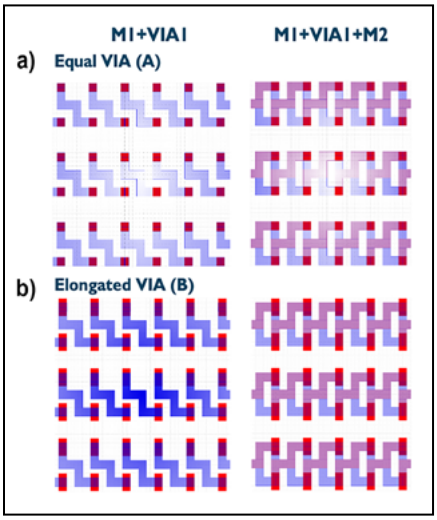

Figure 8: Layout of the RDL stack with two VIA strategies: a) (top) A; and b) (bottom) B.

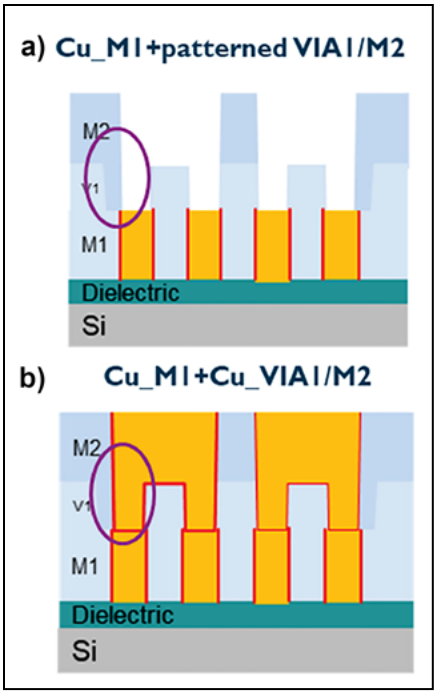

Figure 9: Schematic of M2 to VIA1 truncations: a) (left) Before; and b) (right) After metallization.

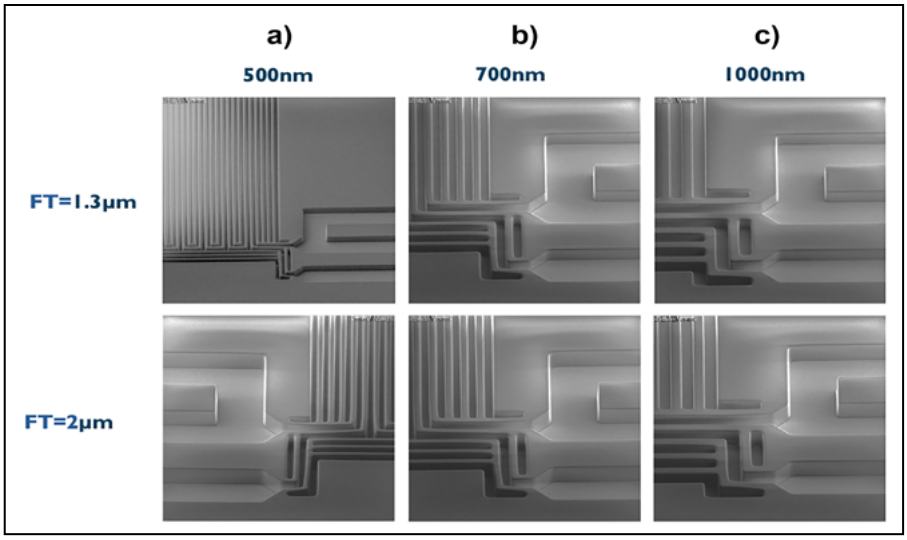

Figure 10: Tilted SEM images of M1 meander-fork structures: a) (left) 500nm; b) (middle) 700nm; and c) (right) 1000nm, post-polymer cure for both FT=1.3µm/and 2.0µm.

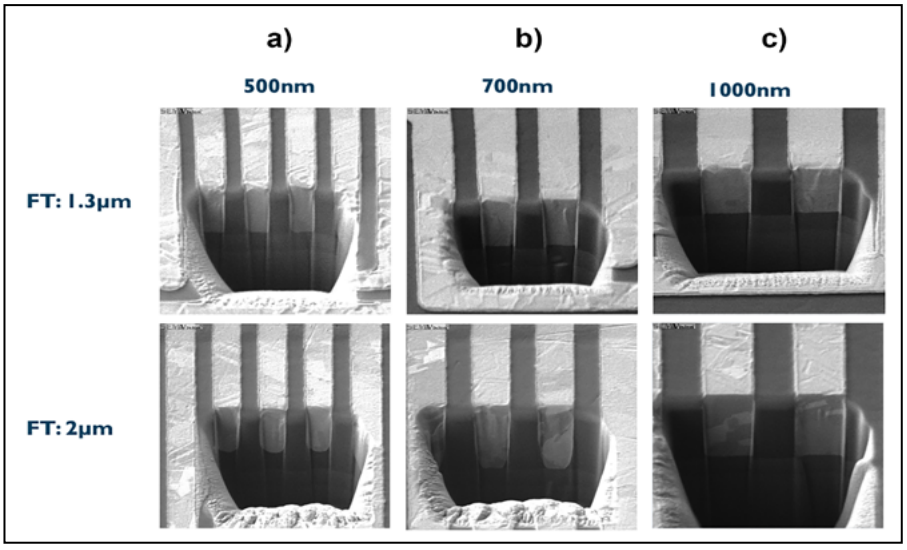

Figure 11: FIB and tilted SEM images of M1 meander-fork structures: a) (left) 500nm; b) (middle) 700nm; and c) (right) 1000nm, post CMP.

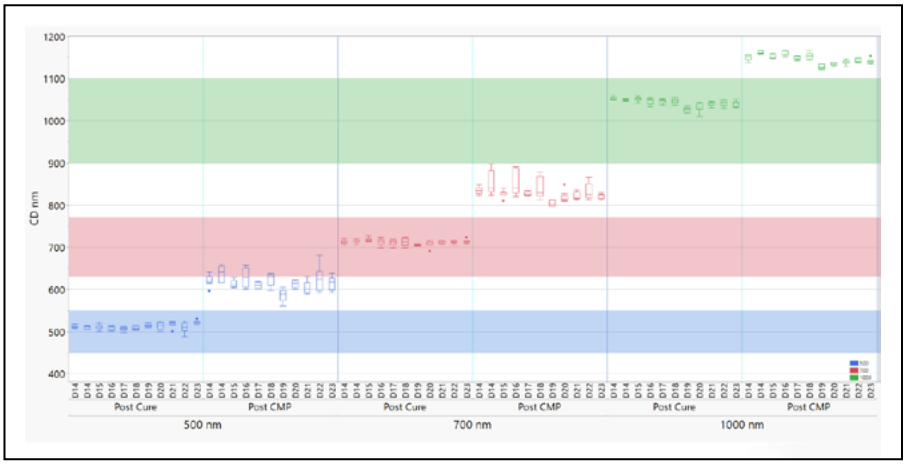

Figure 12: Intra-wafer and wafer-to-wafer CD variance measurements of M1 after development.

Besides the designed two via types, a strategy of enlarging the VIA structures was performed. This was achieved by a deliberate under-exposing of the polymer, thereby enlarging CDs for all structures by 200nm. For the 500nm vias, this corresponds to a 40% increase. The M2 dimensions are still defined as nominal and will truncate the VIA1 openings as exemplified in Figure 9.

Critical dimensions. Figure 10 shows tilted SEM images of the M1 meander-fork structures post-polymer cure. Here we can observe the well-defined patterning of the lines with vertical sidewalls. It can be observed that for the smaller 500nm/700nm structures, the corners suffer a slight deformation with curing, thereby bending the corner inwards. In Figure 11, we confirm again the verticality of the same meander-fork structures post CMP. There are two noteworthy items visible in these focused ion beam (FIB) cuts. The first item corresponds to deviations from verticality for the smaller structures in the 2.0µm film thickness case. The 700nm structures demonstrate a rounder footing, while the 500nm lines are not completely patterned for the entire film thickness. The film thickness/CD aspect ratio (AR) above 3 starts to be too aggressive for this material. The second item pertains to the visible top rounding of the patterned polymer both post cure and post CMP. It becomes apparent that a longer polish is necessary to obtain the desired line width as designed. Intra-wafer and wafer-to-wafer variances were monitored with post-cure CD results within the nominal ±10% range for each structure (Figure 12). Post-CMP results present ~100nm larger CDs.

For the VIA1 layer, the via openings contact the underlying M1 layer. This contact needs to be residue free and the oxide from the Cu RDL needs to be removed and maintained in a vacuum until seed layer sputtering in order to achieve low contact resistance. Polymers and resists typically have a descum (O_2 ashing) to remove residues and reduce footing after development. As via diameters scale smaller, the CD impact of the descum process becomes more important to control and reduce. The descum process is very isotropic. At the sub-micron scale, the corners become rounder and underlying Cu oxide becomes slightly more oxidized. Figure 13 shows top SEM images of the same via at each process stage. Immediately after development, some residues are observable—namely on the smaller 500nm vias.

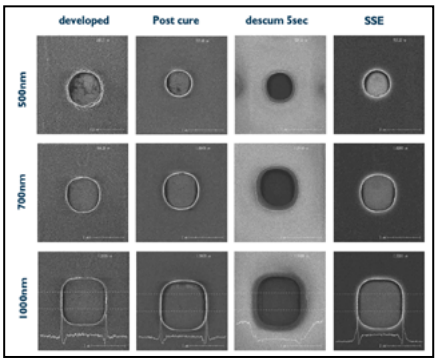

Figure 13: Top-down images of VIA1 after development, cure and two distinct etches.

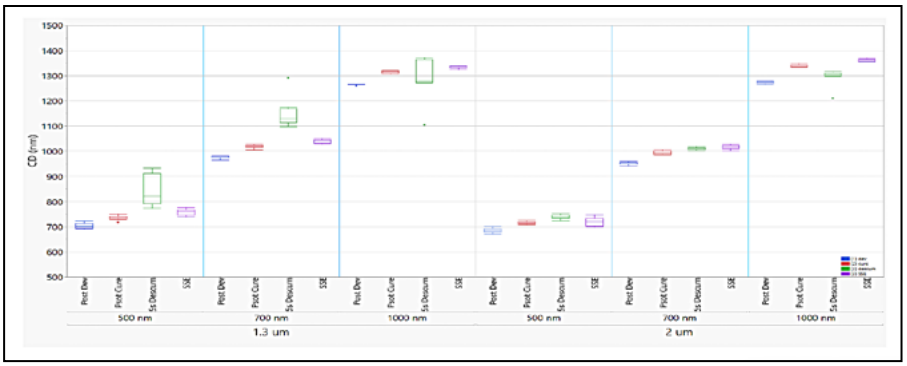

Figure 14: Evaluation of VIA1 CD evolution with different processes.

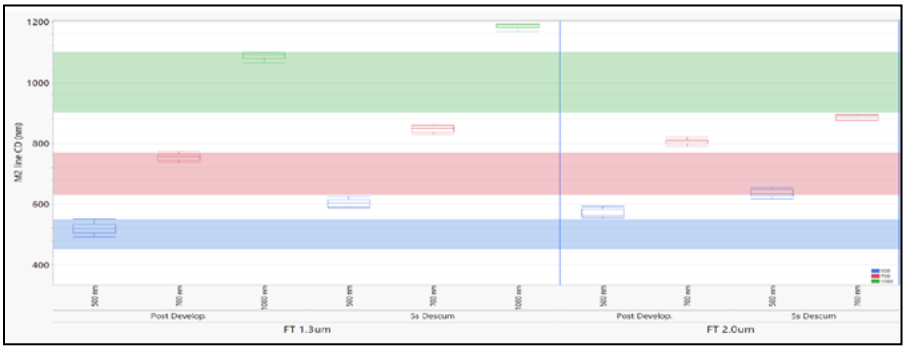

Figure 15: CD measurements of M2 after development and descum.

A small evaluation was conducted, involving either a reduced 5s descum, or a soft sputter etch (SSE). In this evaluation, the SSE image was obtained from a separate wafer. Both the 5s descum and SSE visually eliminated visible residues. However, the descum sample exhibited greater edge rounding and copper oxidation, whereas the SSE wafer showed no visible residues.

Figure 14 presents the critical dimension (CD) measurements of the vias at each stage of the evaluation. The increased edge rounding and lower contrast in the descum samples made their CD measurements more challenging and prone to error. It is unclear whether the reduced descum offers superior performance in residue removal—maintaining the same critical dimension (CD) loss—when compared to the SSE. What is evident is that SSE does not exhibit the top-edge rounding observed with the descum process, nor does it induce copper oxidation. The extended SSE presents itself as a promising candidate for residue removal in a polymer damascene process, particularly given the polymer/barrier polish at the final stage. Further investigation is required.

For the M2 layer, it was decided to perform only the reduced 5s descum process. Figure 15 shows the acquired line width CD measurements both post development and post descum.

Overlay. As structural scaling progresses, the strain on intralayer overlay is expected to intensify. Figure 16 presents the results of overlay monitoring for VIA1-to-M1 and M2-to-VIA1 layers. The measured overlay values ranged from -80nm to 40nm, remaining well within the operational capabilities of the fabrication tool.

The top SEM images presented in Figure 17 demonstrate that the enlarged via strategy aids in maintaining contact with the underlying M1 Cu line; however, it is insufficient to achieve low variance in the contact area. Improved overlay performance is essential to expand the process window and reduce process variability. While the elongated via (Via B) offers benefits by simplifying the via formation process, the length:width=2:1 aspect ratio of the

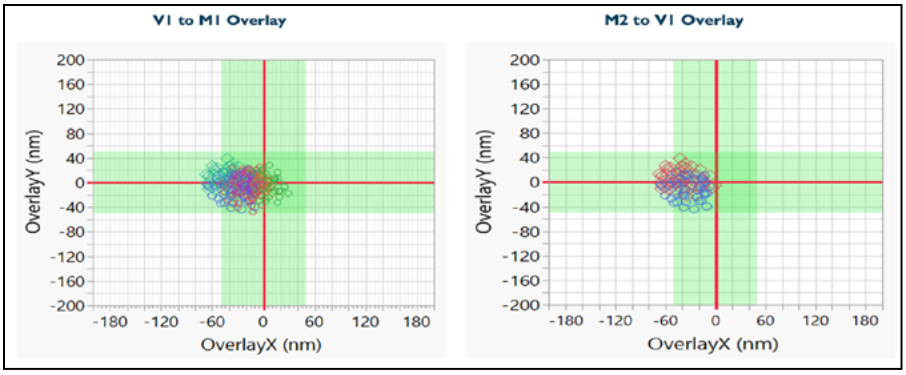

Figure 16: Overlay measurements for: a) (left) VIA1-to-M1; and b) (right) M2-to-VIA1.

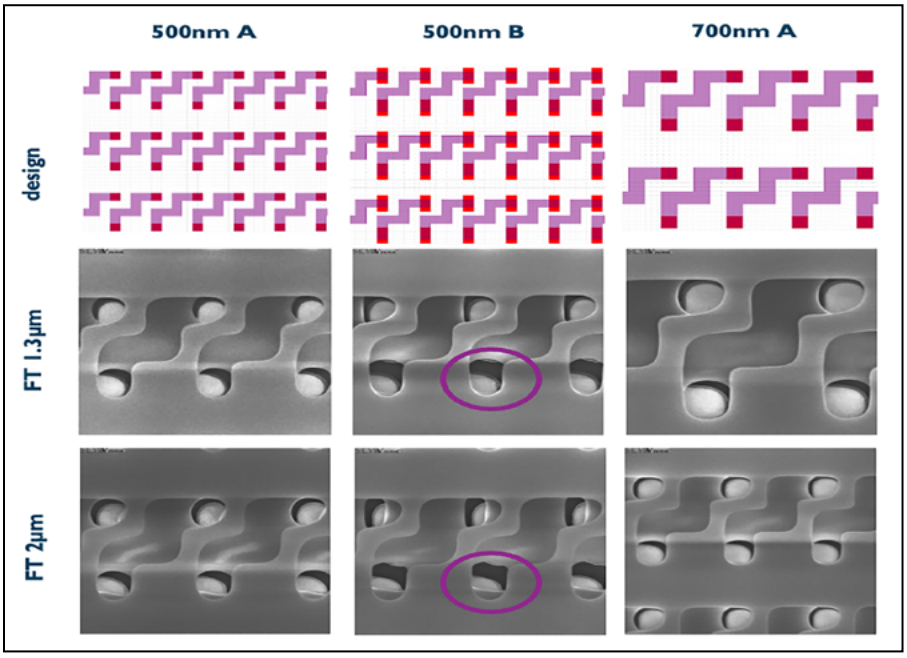

Figure 17: Top SEM images of chain structures with M2 pattering truncating VIA1 layer with visible M1 lines.

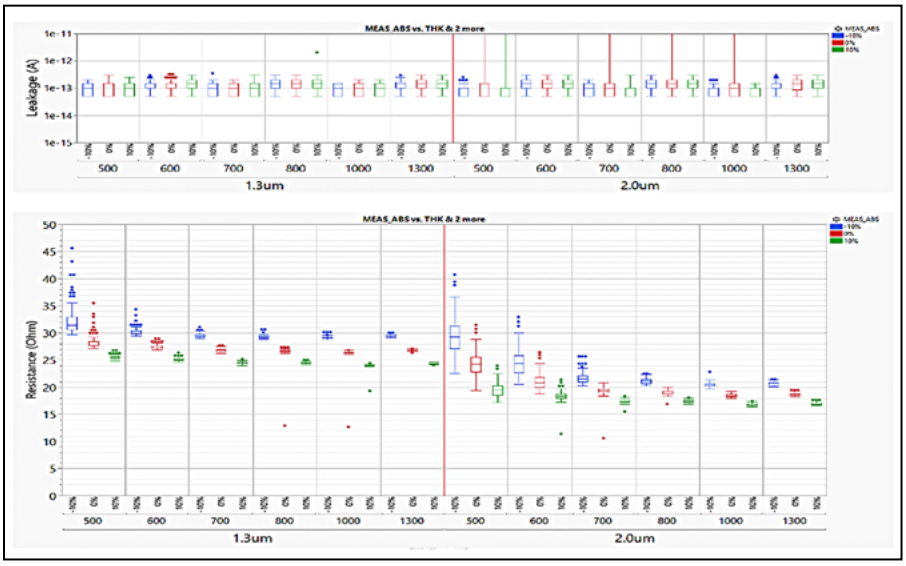

Figure 18: Leakage and line resistance of M1 meander-forks with line CDs ranging from 500nm to 1300nm.

vias is excessive. A more moderate elongation, combined with a small landing pad, is anticipated to enhance process capability (yield) and reduce variability in contact resistance.

Electrical results. Meander-fork test structures are utilized to evaluate M1 and M2 RDL line capability both in terms of leakage and resistance scaling with line CD. In Figure 18 and Figure 19 it can be observed that intra-fork leakage, for an applied voltage of 1V, presents very acceptable values for all CDs and both FTs.

M1/M2 meander-fork line resistance demonstrates full electrical yield for all CDs down to 500nm. For FT=1.3µm, almost perfect linear scaling and low variability were observed across the entire CD range. It can only be said that an increase in variability is beginning to be observed for 500nm. This is to be expected as the material AR for these CDs approaches 3:1. The same is observed for the FT=2.0µm samples. Deviation from linearity and increased variance is observed for CDs smaller than 700nm, AR>3:1. The polymer shows promise of scaling to lower CDs if the AR is maintained below 3:1.

RDL line density is critical for lateral interconnects; however, the area density of vias (vertical inter-layer connections) significantly impacts overall 3D density. Rerouting and reducing RDL lines can become challenging when vias and their respective landing pads are large or numerous. The industry's increasing demand for higher bandwidth necessitates a growing number of chip I/Os, interconnect layers, and faster interconnect speeds. Although bus regions are typically via free, line termination to die contact regions are densely packed. In this context, damascene polymer RDL offers a distinct advantage over semi-additive (SA) RDL strategies, because vias do not require landing pads and are generally smaller in size. In this study, the via critical dimension (CD) matches that of the line CD. To assess process capability, we employed M1-(VIA1)-M2 daisy chain structures with readouts at different block counts (30, 60, 120, 210, 450). Our characterization will focus on line and via CDs of 500nm, 700nm, and 1000nm.

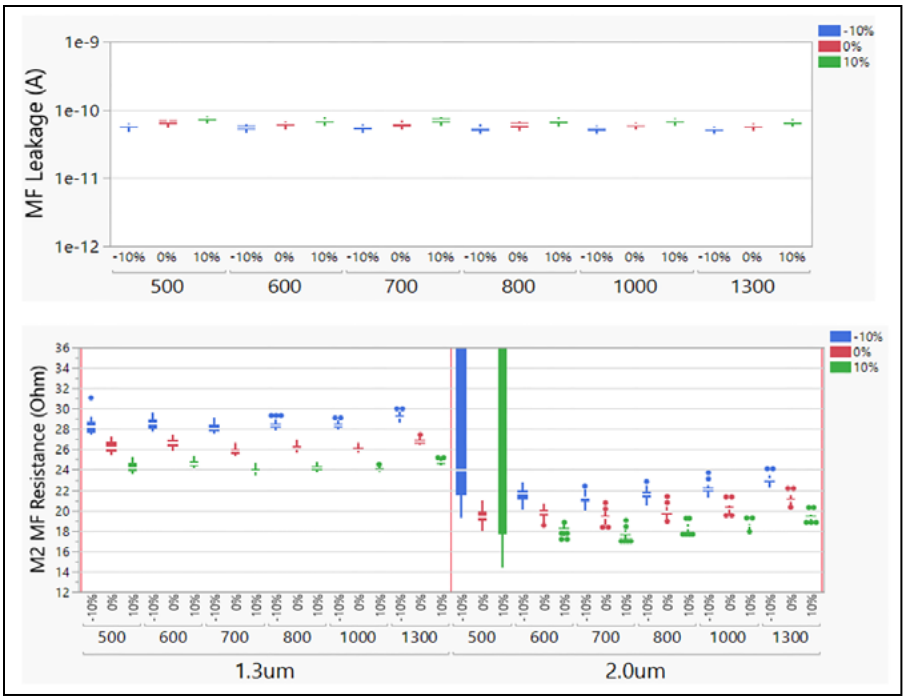

Figure 19: Leakage and line resistance of M2 meander-forks with line CDs ranging from 500nm to 1300nm.

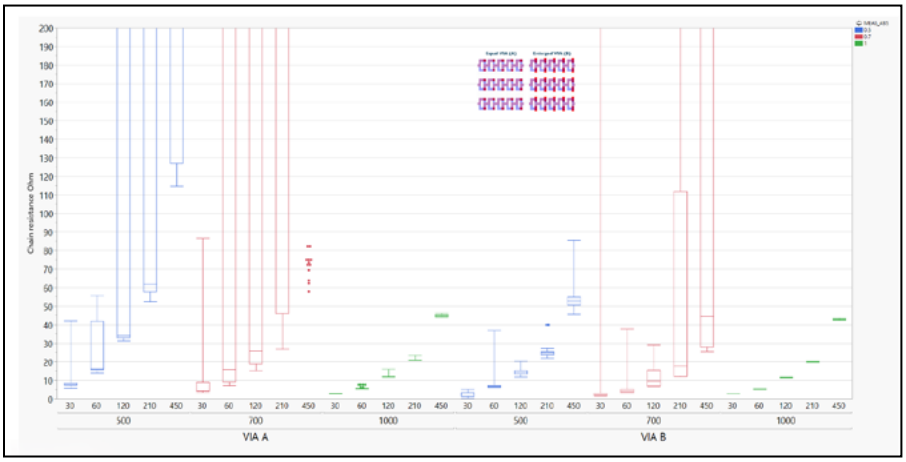

Figure 20: M1-VIA1-M2 (FT=1.3µm) chain resistance as a function of via type, CD, and number of chain blocks.

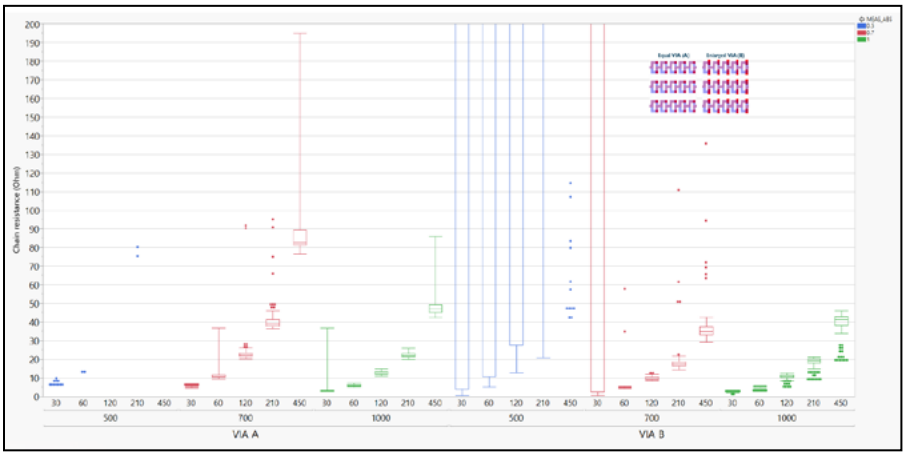

Figure 21: M1-VIA1-M2 (FT=2.0µm) chain resistance as a function of via type, CD, and number of chain blocks.

Figure 20 and **Figure 21** show chain resistance as a function of via type, film thickness, and line/via CD. For FT=2.0µm we have full yielding and low variability results for 700nm and 1000nm structures. Although for elongated vias and 500nm CDs we have yielding structures, the thickness to CD AR is too aggressive. For FT=1.3µm, 1000nm structures are fully yielding and of low variability. The structures of 500nm and 700nm are almost fully yielding, but some variance is observed. Elongated type B vias show better process capability relative to type A. Although this assists in mitigating the overlay and contact area variance, better overlay capabilities are still deemed necessary for fully yielding and low variance.

A FIB cut was performed on an M1-(VIA1)-M2 chain section of type A via and FT=1.3µm. Top SEM and tilted SEM images of the FIB cut are presented in **Figure 22**.

Summary

A new polymer setup was performed successfully targeting better line definitions and higher resolution. The new material demonstrates fully-functional electrical performance with low variability for multilayer fine-pitch polymer damascene RDLs with line/space dimensions reaching 500nm (pitch of 1000nm). In addition, via patterning with CDs down to 500nm (2000nm via to via pitch) was enabled. A strategy of both elongated vias and enlarged vias was implemented, resulting in fully-functional 700nm daisy chains (450 chain blocks) for FT=2.0µm and almost fully-functional daisy chains for 500nm and 700nm for FT=1.3µm. Both elongated and enlarged via strategies assist in mitigating via overlay and contact area variance. Further work, however, is necessary to tune these strategies together with the need for better overlay capabilities to obtain a fully-yielding process.

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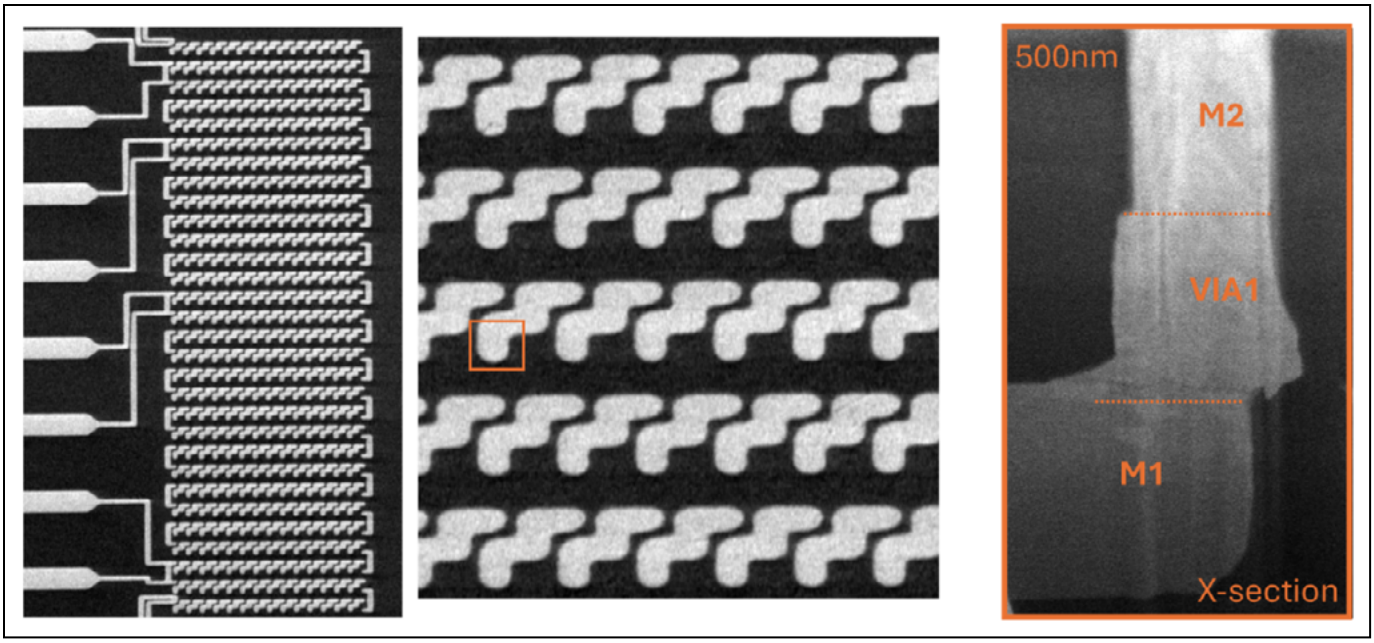

Figure 22: FIB cut and tilted SEM of the 500nm M1-(VIA1)-M2 stack for type A via and FT=1.3µm.

this study. Special thanks to the imec process assistants for the excellent multiple request support. We would also like to express thanks for our ongoing collaboration with JSR Corporation and JSR Micro N. V.

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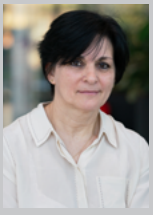

Biographies

Carine Gerets is a Development Engineer in the 3D System Integration Group at imec, Leuven, Belgium. She began her career in the chemical industry and later joined imec where she has contributed to numerous research topics including stacking die and wafer thinning, large die and multi-die stacking, die-to-wafer (D2W) bonding and various 3D packaging methods. She is now focused on screening dual-damascene process materials for FPRDL. She holds a professional Bachelor's degree in Chemistry. Email Carine.Gerets@imec.be

Eric Beyne is a Senior Fellow, VP R&D and Program Director of 3D System Integration at imec, Leuven, Belgium. He has been with imec since 1986, working on advanced packaging and interconnect technologies and holds a degree in Electrical Engineering (1983), and a PhD in Applied Sciences (1990), both from the KU Leuven, Belgium.

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HETEROGENOUS INTEGRATION:
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Highlights of the 26th EPTC Conference

The 26th IEEE Electronics Packaging Technology Conference (EPTC2024), organized by the IEEE Singapore RS/EPS/EDS Chapter and co-sponsored by the IEEE Electronics Packaging Society (EPS), continues to serve as a premier international conference in the Asia-Pacific region, covering the entire spectrum of electronics packaging technology. It is the flagship conference of EPS in the Asia and Pacific Region.

EPTC2024 was held from December 3 to December 6, 2024, at the Grand Copthorne Waterfront Hotel, Singapore. After successfully transitioning back to an in-person format in previous years, EPTC2024 saw an even stronger turnout, with over 650 attendees from across the world representing academia, industry, and research institutions.

The conference featured a rich technical program, with multiple keynote sessions, panel discussions, professional development courses (PDCs), technical tracks, workshops, and networking events. The event provided a platform for experts to exchange insights on all aspects of microelectronics packaging including advanced packaging, heterogeneous integration, interconnect technologies, AI hardware, thermal management, power electronics, wafer-level packaging, and smart manufacturing.

Keynote sessions: Industry leaders shaping the future of packaging

EPTC2024 hosted six keynote speakers, who shared their perspectives on the latest advancements and challenges in semiconductor packaging:

- Calvin Cheung (VP, ASE Inc.): "Advanced Packaging for AI Performance and Power Efficiency,"
- Glenn G. Daves (Senior VP, NXP Semiconductors): "Packaging at the Emerging Edge,"


Calvin Cheung


Glenn G. Daves


Tim Olson


Yu-Po Wang


Devan Iyer


Subramanian S. Iyer

- Dr. Yu-Po Wang (VP, Siliconware Precision Industries Co., Ltd.): "Breaking Boundaries of IC Packaging through Innovative Integration Technology,"
- Tim Olson (CEO, Deca Technologies): "Tectonic Forces Shaping the Future of the Semiconductor Industry,"
- Dr. Devan Iyer (Chief Strategist, IPC International): "Advanced Packaging – Customization Trends and Standardization Opportunities," and
- Prof. Subramanian S. Iyer (Distinguished Professor and the Charles P. Reames Endowed Chair, UCLA): "Strategic Directions for Electronics Packaging."

These keynote sessions highlighted the increasing demand for heterogeneous integration, AI-driven packaging advancements, and sustainability considerations in semiconductor manufacturing.

Emerging industry trends and challenges

EPTC2024 featured two high-profile panel discussions that tackled pressing topics in the semiconductor industry by distinguished industry leaders:

- **Enhancing Southeast Asia's Strategic Role in the Semiconductor Supply Chain:** Moderated by Keat Yap (Kearney), this panel featured experts from Lam Research, Kulicke & Soffa, SSMC, STMicroelectronics, and SSIA. Discussions centered on the region's growing importance in the semiconductor value chain, talent development, and supply chain resilience.
- **Co-Packaged Optics (CPO) for AI Data Centers**: Moderated by Matt Kelly and Devan Iyer (IPC International Inc.), this panel included experts from Marvell, Huawei, UCLA,

Panel Discussion: Enhancing Southeast Asia's Strategic Role in the Semiconductor Supply Chain. Moderated by Keat Yap of Kearney.

Panel discussion: Co-Packaged Optics (CPO) for AI Data Centers. Moderated by Matt Kelly and Devan Iyer of IPC International.

ASE, and Lightspeed Photonics, who discussed AI-driven optical interconnects and the future of high-performance computing.

Professional Development Courses (PDCs) and Workshop

The Professional Development Courses (PDCs) covered six key areas, providing valuable insights into chiplet integration, photonics, wafer bonding, AI & HPC, solder joint reliability, and failure analysis:

1. Chiplet, Heterogeneous Integration, and Co-Packaged Optics, John H Lau.
2. Photonic Technologies for Communication, Sensing, and Displays, Torsten Wipiejewski.
3. Wafer Bonding for Advanced Packaging Applications, Viorel Dragoi.
4. Current and Future Challenges and Solutions in AI & HPC System and Thermal Management, Refai-Ahmed Gamal.
5. Mechanics and Reliability of Lead-Free Solder Joints, Jeff Suhling.
6. Failure Analysis of Advanced Packages: Fundamental, Skills, Philosophy and Case studies, Yong-Fen Hsieh.

Additionally, a dedicated **Heterogeneous Integration Workshop** was convened where global experts from academia and industry discussed the latest technological developments

Heterogeneous Integration Workshop.

EPS Student Travel Grants awards.

Exhibitors at the 26th EPTC Conference.

and collaborative opportunities in next-generation semiconductor packaging.

Technical program: Cutting-edge research and innovations

EPTC2024 showcased an extensive technical program, with multiple tracks and oral presentations covering:

- Advanced Packaging & Heterogeneous Integration
- Interconnect Technologies & Thermal Management
- 2.5D/3D Integration, TSV, and Wafer-Level Packaging
- Smart Manufacturing, Reliability, and Failure Analysis
- Materials, Processing, and Characterization
- Automotive & Power Electronics Packaging
- Wireless & Antenna Packaging, and Emerging Technologies

An interactive poster session further enriched the experience, offering in-depth discussions on key packaging challenges and solutions.

Exhibition and networking and opportunities

EPTC2024 also provided ample networking opportunities, including a well-attended industry exhibition at the Waterfront Foyer featuring 21 exhibitors, 16 sponsors, and 7 conference partners. Attendees engaged in sponsor presentations, live demonstrations, and technology showcases.

One of the highlights of the conference was the EPS Luncheon, where EPS President-Elect Prof. Jeff Suhling delivered a welcome speech. Certificates of appreciation were awarded to members of the Organizing Committee, and the EPS R10 Regional Contributions Award was presented to Yik-Yee Tan. Additionally, EPS Student Travel Grants were awarded to nine outstanding students from universities across Japan, the USA, France, China, and India, reinforcing EPS's commitment to fostering young talent in electronics packaging.

A banquet dinner at RedDot BrewHouse, Dempsey Hill offered a relaxed environment for attendees to connect, fostering new collaborations in the field.

Closing Ceremony

EPTC2024 concluded with best paper awards, sponsor recognitions, and an invitation to EPTC2025, which will take place from December 2–5, 2025, in Singapore. The conference reaffirmed its status as a key platform for knowledge exchange, industry-academia collaboration, and innovation in semiconductor packaging technology.

For further updates, visit the EPTC website: www.eptc-ieee.net.

ECTC 2025 – Leading-edge packaging and component breakthroughs pushing the scale of connectivity

This year's conference celebrates 75 years of success in helping the microelectronics industry move forward

By Przemyslaw Gromala [75th ECTC Program Chair]

On behalf of the Program and Executive Committees, I invite you to attend the 75th anniversary IEEE Electronic Components and Technology Conference (ECTC), May 27–30, 2025 at the Gaylord Texan Resort & Convention Center in Dallas, TX. The 75th anniversary of this premier event, sponsored by the IEEE Electronics Packaging Society, brings together more than 2,000 professionals from across the global microelectronics packaging industry, including manufacturers, design houses, foundries, material suppliers, universities, and investors. Join us to connect with key stakeholders and explore cutting-edge advancements in the field.

Gaylord Texan Resort & Convention Center in Dallas, TX.

ECTC began in 1950 as the Symposium on Improved Quality Electronic Components, held at the U.S. Department of the Interior and sponsored by the former American Institute of Electrical Engineers (AIEE), Institute of Radio Engineers (IRE), and Electronic Industries Association (EIA). In succeeding years the conference has evolved in many ways, with various name changes, technical programs aligned with evolving electronics technologies, different locations and co-sponsors. Today, the ECTC conference serves as a global platform for exploring leading-edge advancements in microelectronic packaging and component technologies, fostering innovation, and addressing industry challenges.

Keynote talk on criticial technologies for zettascale computing

On Wednesday, May 28, Samuel Naffziger, Sr. Vice President and Corporate Fellow at AMD, will deliver a keynote talk on Achieving Efficient Zettascale Computing in the AI Era, addressing the urgent need for scalable, energy-efficient computing solutions.

The demand for computing power and energy is increasing rapidly, driven by the fast expansion of artificial intelligence (AI). Meeting this challenge requires innovation across the entire computing stack, from devices to datacenters. A key approach involves integrating domain-specific accelerators with advanced 2.5D and 3.5D packaging to maximize compute density and efficiency. These accelerators, combined with other system components, must be assembled into tightly integrated SLEDS that minimize power loss and optimize high-speed communication through workload-aware power management. This keynote will explore the critical technologies shaping the future of high-performance computing and the innovations required to sustain its exponential growth.

Samuel Naffziger, Sr. Vice President and Corporate Fellow at AMD.

New special sessions and workshops

The 75th anniversary ECTC conference will introduce several new program events. First, this year there will be 11 special sessions, including nine on Tuesday, each lasting 90 minutes. Tuesday's schedule now includes two sets of parallel sessions instead of one, featuring a rich, diverse offering of compelling topics and expert panelists.

Topics covered throughout the day include: Ultra High-Density Interconnect Technologies, Hybrid Bonding, Quantum Advanced Packaging, and a Comparison of Glass Core vs. RDL Interposers. In the afternoon, additional sessions will focus on Advanced Materials for Co-Packaged Optics and Fault & Failure Analysis in Chiplets. The final set of sessions includes discussions on Sub-THz Packaging for Communication and Radar, as well as Thermal Management for Power Delivery.

Running parallel to these sessions, the Heterogeneous Integration Roadmap (HIR) workshop will feature four focused discussions: IoT & AI at the Edge, Advancing Heterogeneous Integration through Metrology & AI, Integrating Photonics in HPC & Network Systems, and Advances in Panels, Substrates, and Printed Circuit Boards.

On Thursday, May 29, ECTC will feature a Plenary Session on Emerging Advanced Power Delivery for the AI Computing Era. On Friday, an IEEE EPS President's panel will discuss the Challenges and Benefits of Recruiting and Retaining a Diverse Workforce.

Lastly, the Thursday ECTC Reception Gala will be expanded with a special event to celebrate the conference's 75th anniversary.

Workforce development and student outreach

To support workforce development, ECTC is launching a new student engagement program, partnering with local universities and colleges to invite approximately 20 undergraduate students on Wednesday, introducing them to the fascinating world of microelectronics packaging and technologies.

Additionally, this year features a student competition challenge. Three winning teams will be invited to the conference to present their projects during Pitch Night, co-organized with the Start-Up Competition Challenge.

Networking opportunities and ITherm courses

Tuesday evening offers networking and professional engagement opportunities, including a Young Professionals Networking Event featuring a new fishbowl discussion format. This will be followed by an IEEE EPS Seminar on User Perspectives of Chiplet Technology.

Additionally, the IEEE ITherm Conference, co-located with the 75th Anniversary ECTC, will co-organize 16 CEU-approved Professional Development Courses (PDCs) on Tuesday, May 27, offering expert-led training on various topics.

A large and comprehensive technical program

At the 75th ECTC, approximately 400 technical papers will be presented in 36 oral sessions and five interactive sessions. Authors from more than 20 countries will share their latest research on topics including: 3D integration, bridge and chiplet integration, hybrid bonding, wafer-to-wafer and chip-to-wafer bonding, novel substrate materials, high-density RDL, next-generation interconnections, warpage management of large panel, and large-package manufacturing, additive manufacturing, wearable and medical applications, AI/machine language (ML), and advanced RF and antenna designs, thermal management, interconnect reliability, advanced characterization, and process simulations, eco-friendly packaging and secure designs. Interactive sessions will focus on innovations in bonding, power delivery, optimization algorithms, specialized device packaging, and reliability testing.

Exhibits

The ECTC Exhibits on Wednesday and Thursday showcase cutting-edge technologies and products from more than 100 leading companies in electronic components, materials, packaging, equipment and services. Starting daily at 9 a.m., they provide excellent opportunities for networking during coffee breaks, luncheons, and evening receptions.

Whether you are an engineer, manager, student, or executive, ECTC offers unique experiences for everyone in the microelectronics packaging and components industry. We invite you to make plans now to join us for the 75th Anniversary ECTC and to be a part of all the exciting technical and professional opportunities.

I want to thank our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who help make the 75th Anniversary ECTC a success. I look forward to meeting you at the Gaylord Texan Resort & Convention Center, Dallas, Texas, from May 27–30, 2025. Przemyslaw Gromala, 75th ECTC Program Chair. pgromala@ieee.org

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Brewer Science www.brewerscience.com 26
DECA Technology www.thinkdeca.com 30
DL Technology www.dltechnology.com 50
ECTC www.ectc.net 55
EV Group www.evgroup.com 2
FINECS www.finecs.co.jp 16
IMAPS www.imaps.org/page/CHIPcon-2025 58
Ironwood Electronics www.ironwoodelectronics.com 35
ISC CO., LTD. www.isc21.kr ..... IBC
JC CHERRY www.jccherry.com 48
Leeno Industrial www.leeno.com ..... IFC, 37
LPKF Laser & Electronics www.lpkf.com/en 9
MRSI Systems www.mrsisystems.com 32
Nordson Test & Inspection www.nordson.com/testinspect 12, 13
PacTech www.pactech.com 15
Plasma Etch www.plasmaetch.com 27
SEMI 3D & Systems Summit www.semi.org/eu/connect/events/3d-and-systems-summit 55
Smiths Interconnect www.smithsinterconnect.com 29
Sonix www.sonix.com 51
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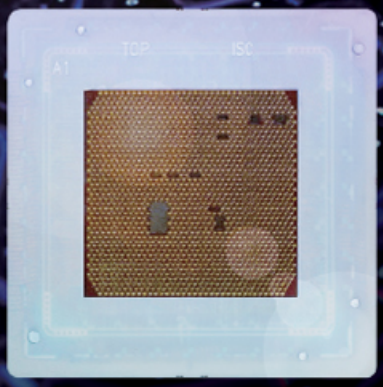

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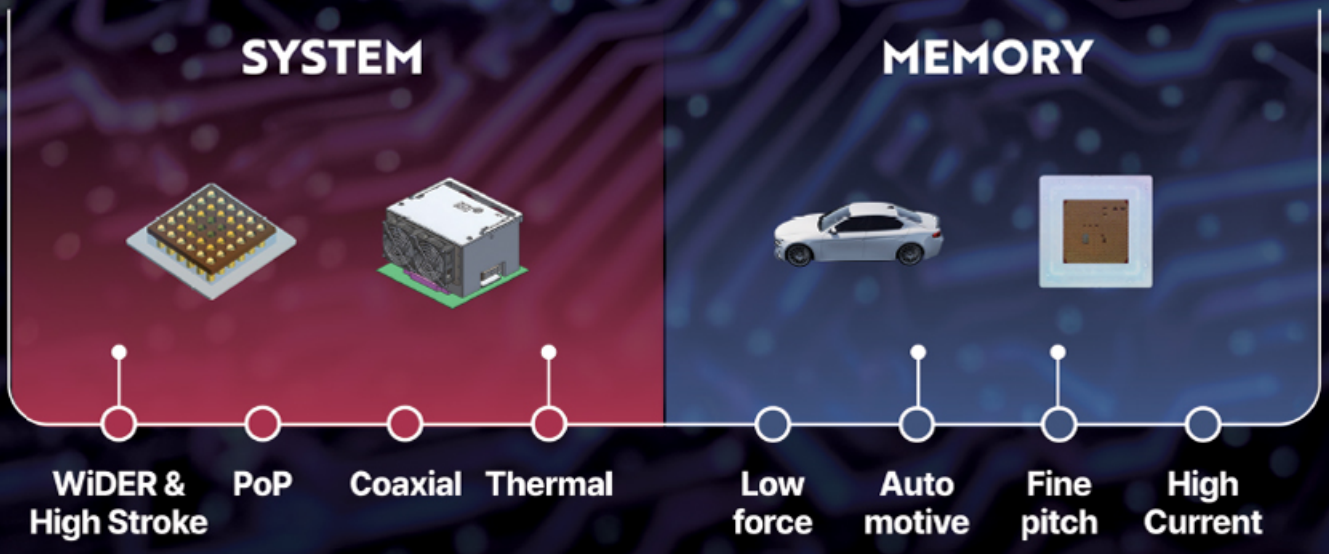

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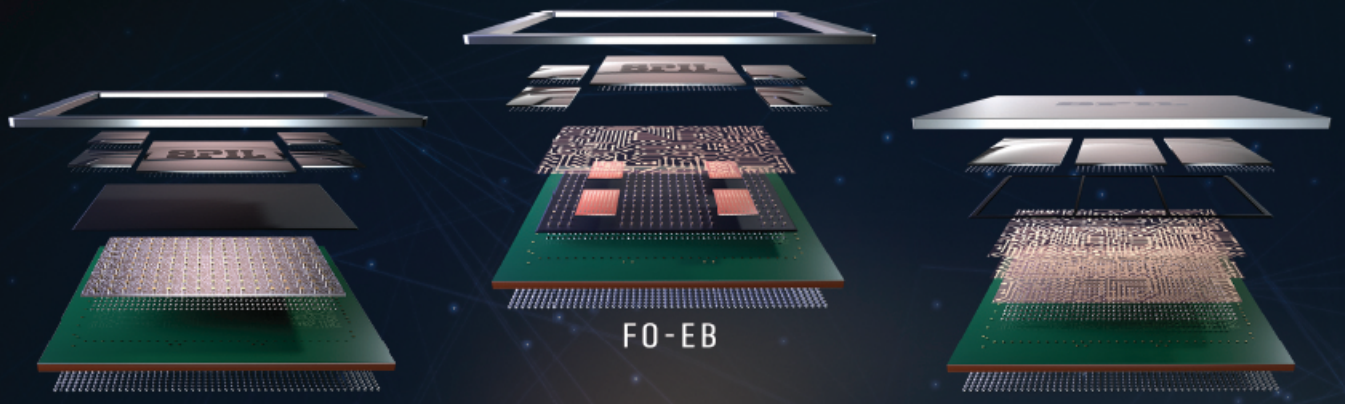

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